

COMPAL CONFIDENTIAL

MODEL NAME : **VAQ10**

PCB NO : **LA-9772P**

BOM P/N : **TBD**

Diesel 15"

REV : **0.1 (X00)**

2014.04.22

@ : Nopop Component

EMC@ : EMI/ESD/RF part

CONN@ : Connector Component

CXDP@,PXDP@ : Total debug Component

X76@,X761@,X76_cap@ : follow X76 group table

GPIO MAP:

ROM part (U52,U53)	Source	X76 P/N	Page
U52:W25Q64FVSSIQ(SA000039A30) U53:W25Q32FVSSIQ(SA00003K820)	main source	X7650731L03	21
U52:MX25L6473EM2I-10G(SA00006N100) U53:MX25L3273EM2I-10G(SA00006N000)	2nd source	X7650731L04	
U52:N25Q064A13ESECOF(SA00005L100) U53:N25Q032A13ESE40F(SA00005KR00)	3rd source	X7650731L05	

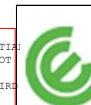
USB3 Re-driver (U638)	Source	X76 P/N	Page
PS8723B (SA000064P10)	main source	X7650931L01	41
PTN36242LBS (SA000060K0L)	2nd source	X7650931L02	

PCIE/SATA Re-driver (U637)	Source	X76 P/N	Page
PS8555BTQFN20GTR2-A0 (SA00006P000)	main source	X7650931L04	44
ASM1467 (SA000068K00)	2nd source	X7650931L03	

Cap. part OSCON Cap.(CD58,CD80) Polymer Cap.(C323,C324,C667)	Source	X76 P/N	Page
CD58,CD80:330uF(SF000003100) C323,C324,C667: 150uF(SGA00003700)	main source	X7650931L09	15,16 40,41
CD58,CD80:220uF(SF000006600) C323,C324,C667: 150uF(SGA20151370)	2nd source	X7650931L10	

MB PCB	
Part Number	Description
DAA0006010	PCB OMF LA-9771P REV1 MB

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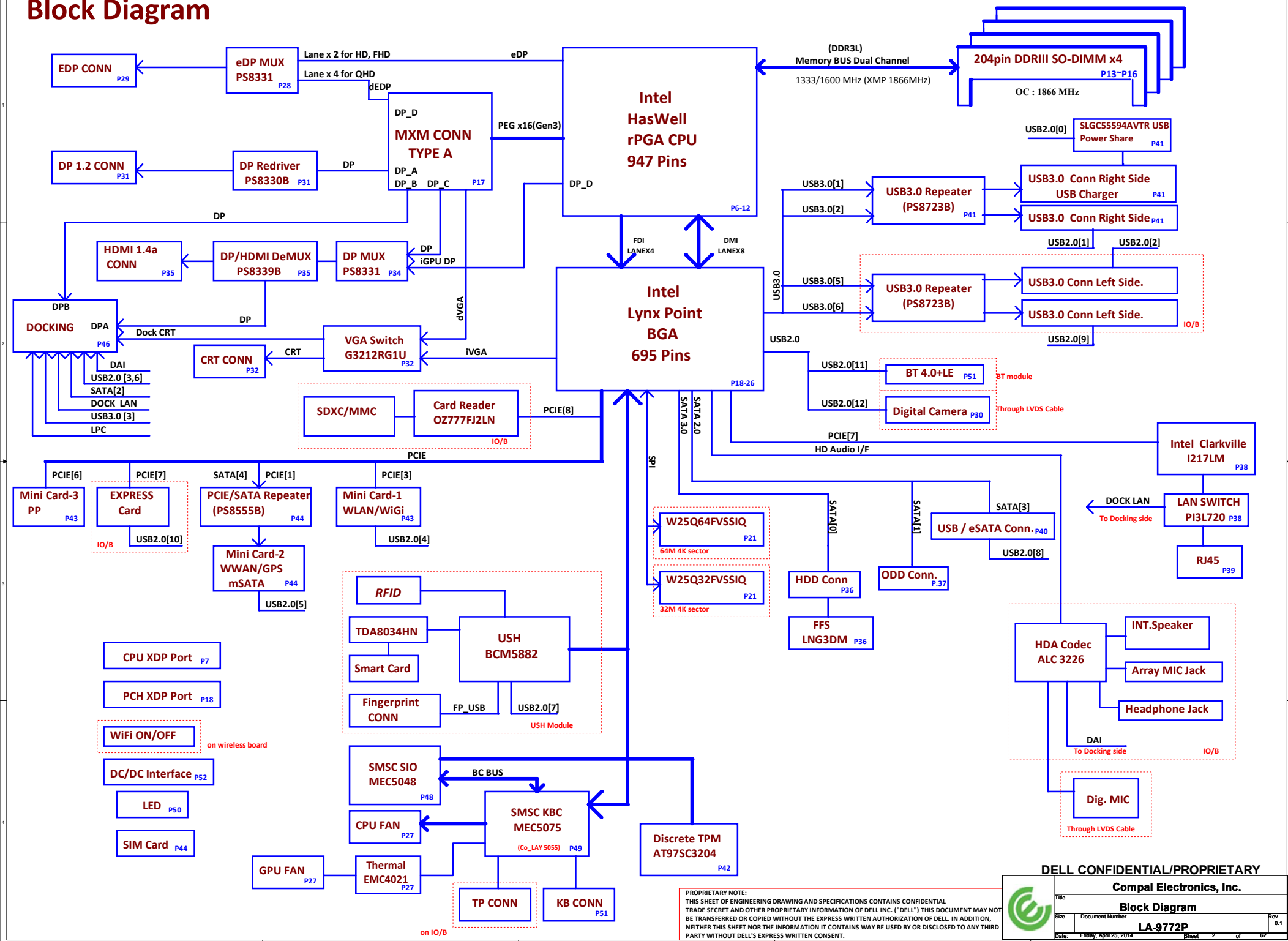


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Block Diagram



POWER STATES

Signal State	SLP S3#	SLP S4#	SLP S5#	S4 STATE#	SLP M#	ALWAYS PLANE	M PLANE	SUS PLANE	RUN PLANE	CLOCKS
S0 (Full ON) / M0	HIGH	HIGH	HIGH	HIGH	HIGH	ON	ON	ON	ON	ON
S3 (Suspend to RAM) / M1	LOW	HIGH	HIGH	HIGH	HIGH	ON	ON	ON	OFF	OFF
S4 (Suspend to DISK) / M1	LOW	LOW	HIGH	LOW	HIGH	ON	ON	OFF	OFF	OFF
S5 (SOFT OFF) / M1	LOW	LOW	LOW	LOW	HIGH	ON	ON	OFF	OFF	OFF
S3 (Suspend to RAM) / M-OFF	LOW	HIGH	HIGH	HIGH	LOW	ON	OFF	ON	OFF	OFF
S4 (Suspend to DISK) / M-OFF	LOW	LOW	HIGH	LOW	LOW	ON	OFF	OFF	OFF	OFF
S5 (SOFT OFF) / M-OFF	LOW	LOW	LOW	LOW	LOW	ON	OFF	OFF	OFF	OFF

PM TABLE

power plane State	+5V_ALW +3.3V_ALW2 +3.3V_ALW_PCH +3.3V_RTC_LDO	+3.3V_SUS +1.35V_MEM	+5V_RUN +3.3V_RUN +1.5V_RUN +0.675V_DDR_VTT +VCC_CORE +1.05V_RUN	+3.3V_M +1.05V_M	+3.3V_M +1.05V_M (M-OFF)
S0	ON	ON	ON	ON	ON
S3	ON	ON	OFF	ON	OFF
S5 S4/AC	ON	OFF	OFF	ON	OFF
S5 S4/AC don't exist	OFF	OFF	OFF	OFF	OFF

USB3.0 PORT	DESTINATION
1	JUSB1 (Ext Right Side)
2	JUSB2 (Ext Right Side)
3	Dock
4	NA(define PCIE_2)
5	IO/B- JUSB1(Ext Left Side)
6	IO/B- JUSB2(Ext Left Side)

PCH	USB PORT#	DESTINATION
	0	JUSB1 (Ext Right Side)
	1	JUSB2 (Ext Right Side)
	2	IO Board- JUSB1 (Ext Left Side)
	3	Docking USB3.0
	4	WLAN/WIGIG
	5	WWAN/GPS/LTE/UWB/mSATA
	6	Docking USB 2.0
	7	USH
	8	ESATA
	9	IO Board- JUSB2 (Ext Left Side)
	10	Express Card
	11	NA
	12	Carmera
	13	NA

USH	0	BIO
	1	NA

Stack up

Layer No.	Name	Er	Material	Thickness (Material SPEC.) Unit : mil	Thickness (Actuality) Unit : mil
			SolderMask	IT-158	0.50
			Add Plating		1.00
1	Top		Copper foil	0.5oz	0.65
		3.7	Prepreg	1080	2.60
2	GND1		Copper foil	1oz	1.35
		3.7	Core	4mil	3.91
3	Sig 1		Copper foil	1oz	1.35
		4.1	Prepreg	2116Mx2	8.26
4	GND/PWR		Copper foil	1oz	1.35
		3.7	Core	4mil	3.91
5	Sig 2		Copper foil	1oz	1.35
		3.8	Prepreg	1080Hx2	4.80
6	Sig 3		Copper foil	1oz	1.35
		3.7	Core	4mil	3.91
7	GND/PWR		Copper foil	1oz	1.35
		4.1	Prepreg	2116Mx2	8.26
8	Sig 4		Copper foil	1oz	1.35
		3.7	Core	4mil	3.91
9	GND 3		Copper foil	1oz	1.35
		3.7	Prepreg	1080	2.60
10	Bottom		Copper foil	0.5oz	0.65
			Add Plating		1.00
			SolderMask		0.50
Overall Thickness (1.45mm ± 10%)				57.09	57.26000
					1.454404

SATA	DESTINATION
SATA 0	HDD1
SATA 1	ODD
SATA 2	Dock
SATA 3	ESATA
SATA 4	mSATA
SATA 5	NA

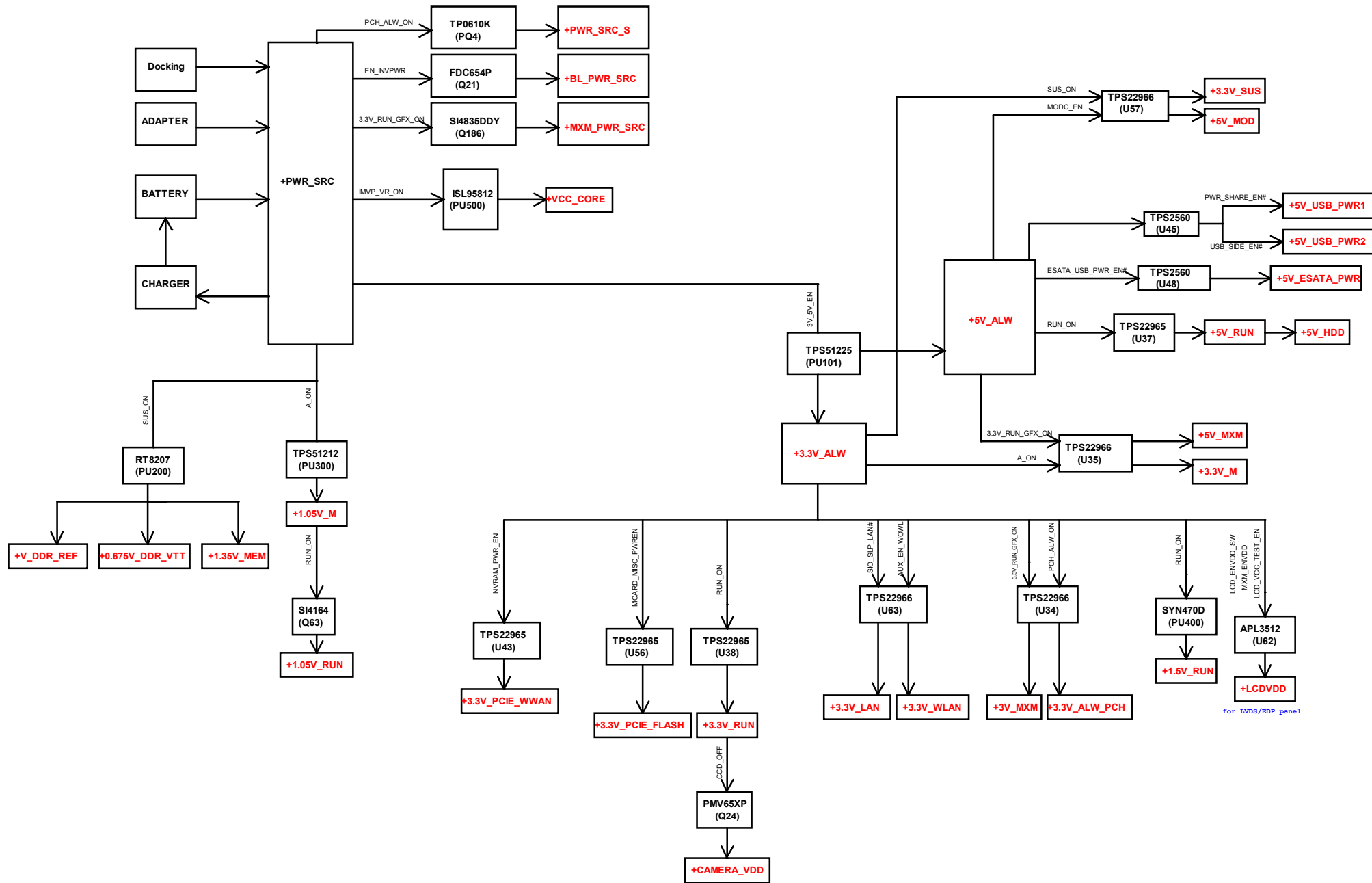
PCI EXPRESS	DESTINATION
Lane 1	mSATA/WWAN
Lane 2	10/100/1G LOM
Lane 3	MINI CARD-2 (WLAN)
Lane 4	NA
Lane 5	NA
Lane 6	MINI CARD-3(PP)
Lane 7	EXPRESS CARD
Lane 8	MMI(Card reader)

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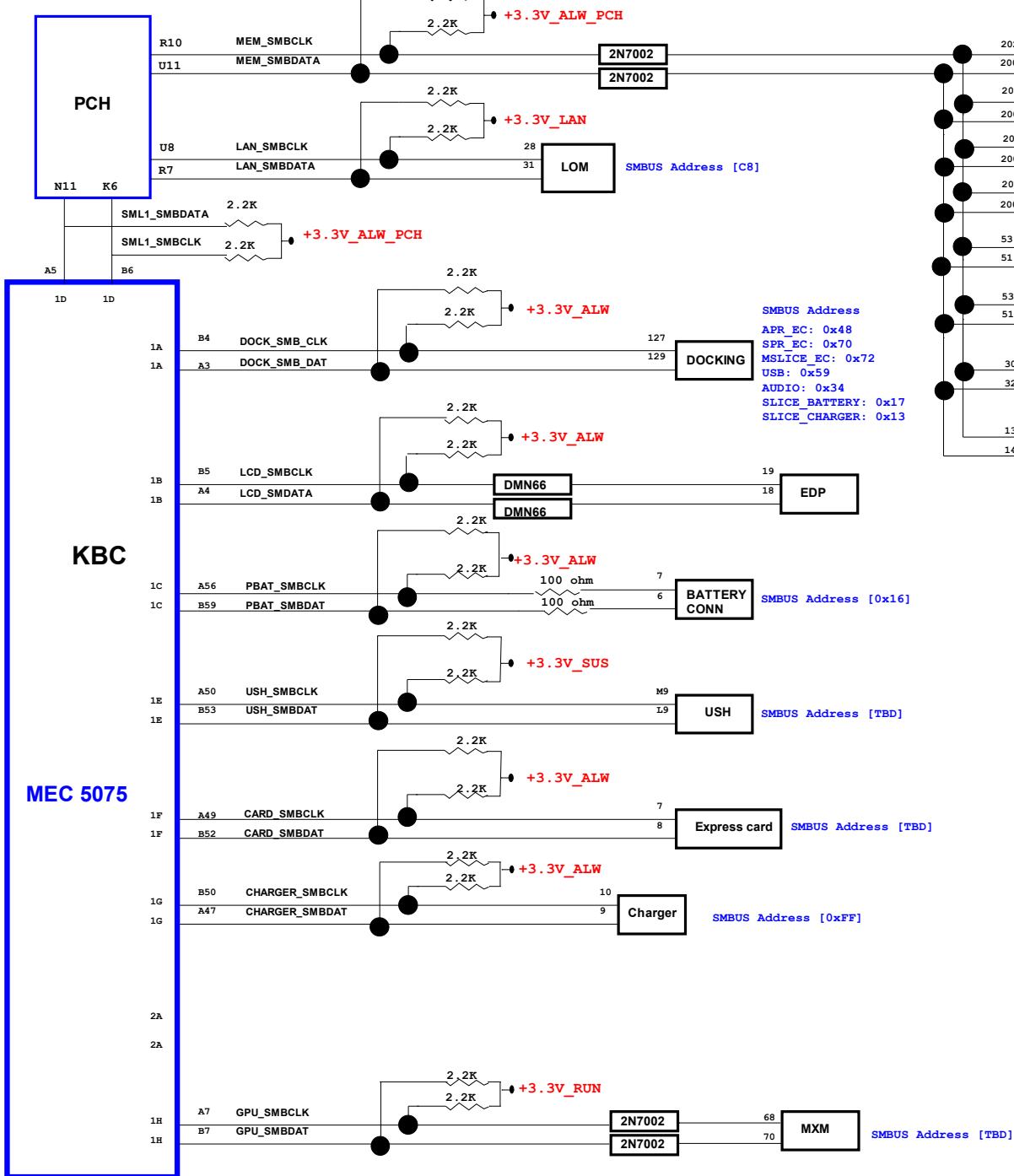
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SMBUS Address [0x9a]



SMBUS Address
SMB_ADM1032: 0x98
SMB_DIAG_DUMP: 0x04
SMB_DIAG_DUMP2: 0x05
SMB_BLACKTOP: 0x60

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SMBUS Bolck Diagram

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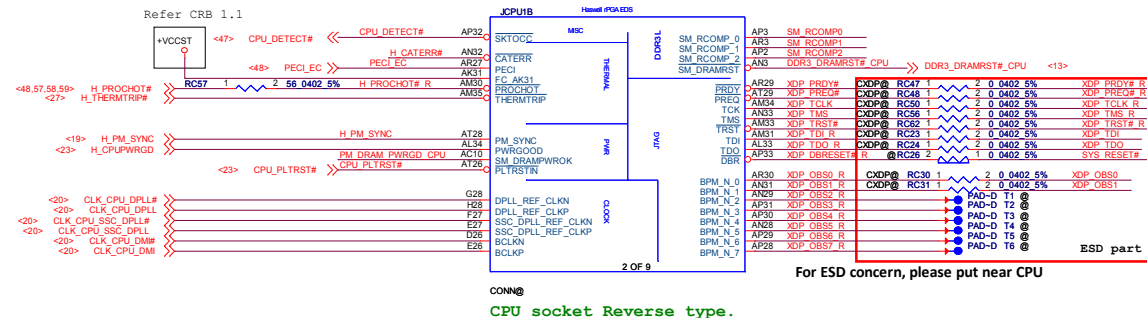
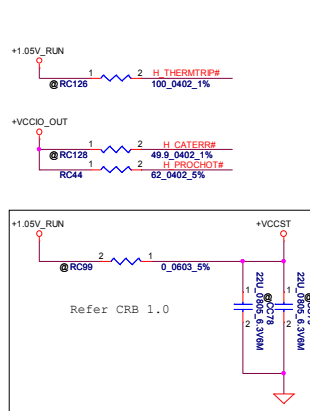
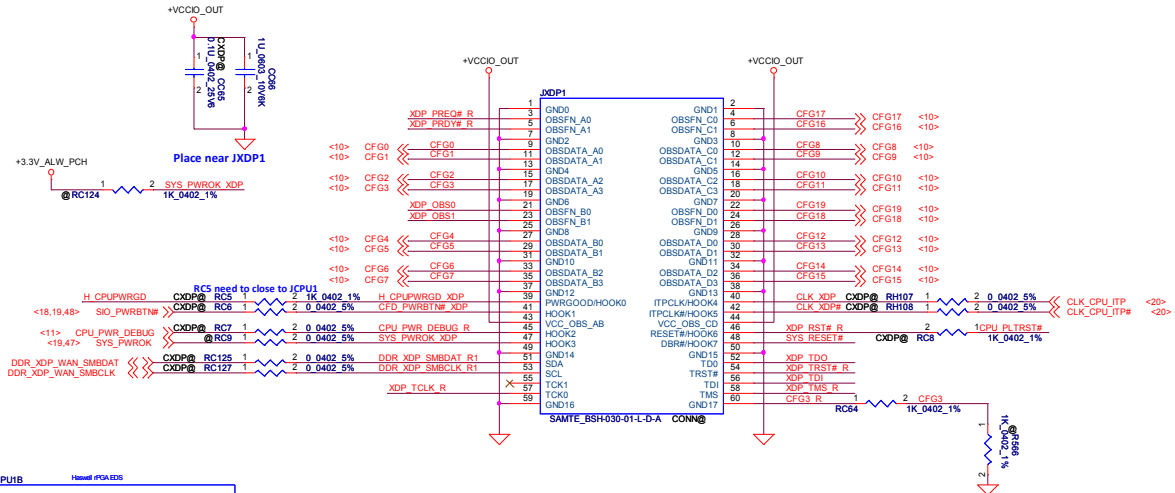
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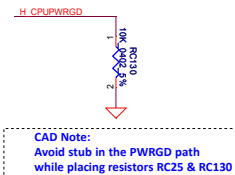
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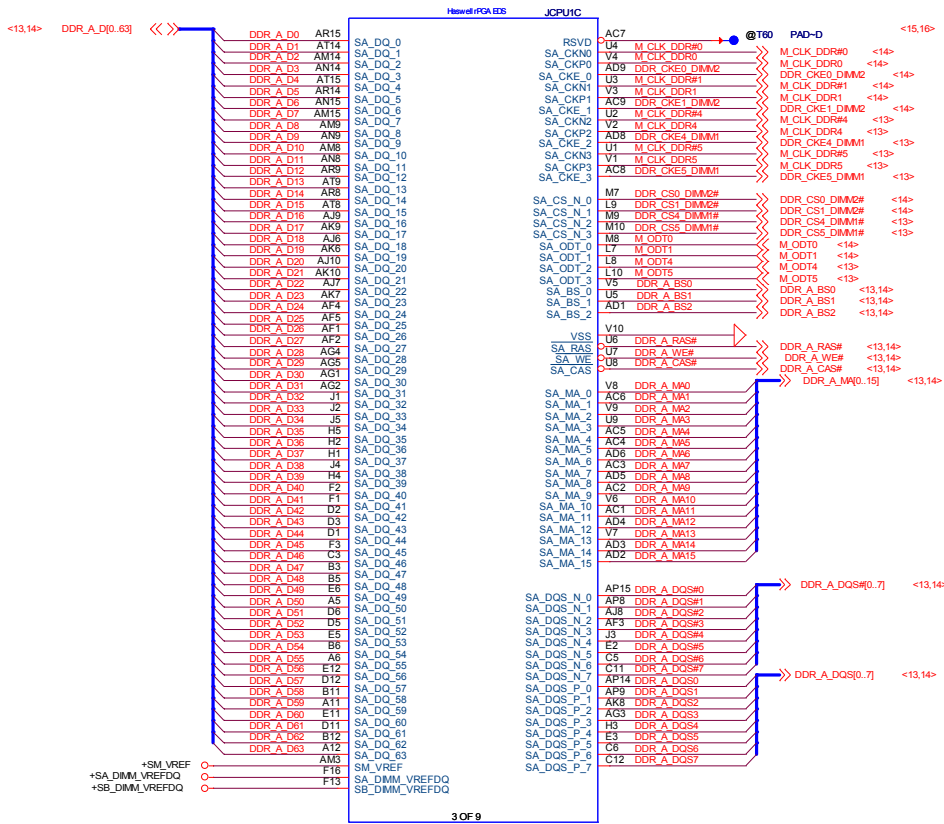
[illegible]

For ESD concern, please put near CPU



CAD Note:
Trace width=12~15 mil, Spacing=20 mils
Max trace length: 500 mil

Timing diagram showing signals XDP_DBRESET# R, XDP_TMS, XDP_TDI R, XDP_PRE0#, XDP_TDO R, XDP_TCLK, and XDP_TRST# over time. The signals are shown as square waves with a period of 1 ns and a duty cycle of 50%. The signals are labeled with their names, pin numbers, and timing parameters. The XDP_DBRESET# R signal is shown with a 100 ns delay. The XDP_TMS signal is shown with a 100 ns delay. The XDP_TDI R signal is shown with a 100 ns delay. The XDP_PRE0# signal is shown with a 100 ns delay. The XDP_TDO R signal is shown with a 100 ns delay. The XDP_TCLK signal is shown with a 100 ns delay. The XDP_TRST# signal is shown with a 100 ns delay. The signals are connected to pins 1, 2, 3, 4, 5, 6, 7, and 8 of the XDP device.



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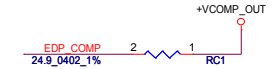
Haswell (3/7)

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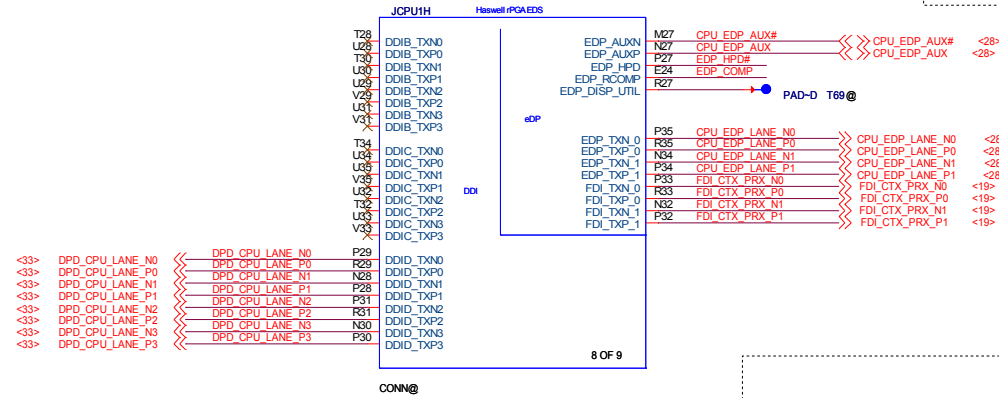
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COMPENSATION PU FOR eDP

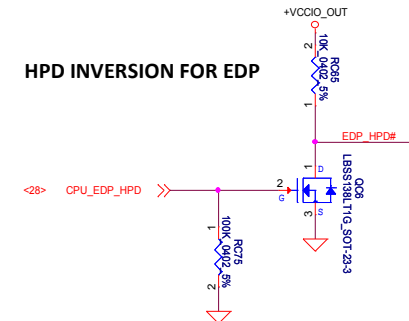


CAD Note: Trace width=20 mils ,Spacing=25mil,
Max length=100 mils.



CPU socket Reverse type.

HPD INVERSION FOR EDP



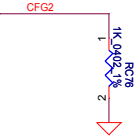
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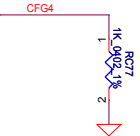
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CFG STRAPS for CPU



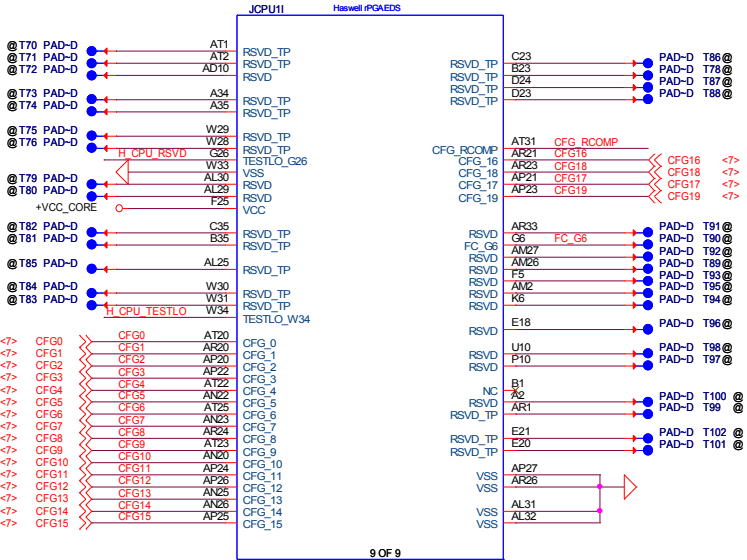
PEG Static Lane Reversal - CFG2 is for the 16x	
CFG2	1:(Default) Normal Operation; Lane # definition matches socket pin map definition 0: Lane Reversed



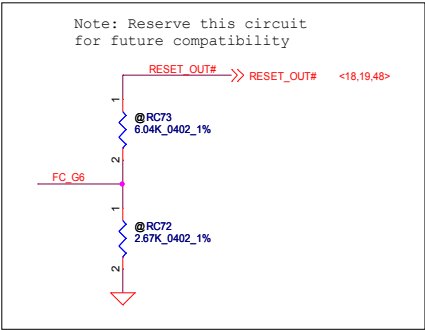
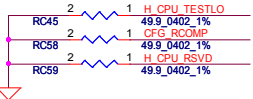
Display Port Presence Strap	
CFG4	1 : Disabled; No Physical Display Port attached to Embedded Display Port 0 : Enabled; An external Display Port device is connected to the Embedded Display Port

PCIe Port Bifurcation Straps(PEG)	
CFG[6:5]	11: (Default) x16 - Device 1 functions 1 and 2 disabled 10: x8, x8 - Device 1 function 1 enabled ; function 2 disabled 01: Reserved - (Device 1 function 1 disabled ; function 2 enabled) 00: x8,x4,x4 - Device 1 functions 1 and 2 enabled

PEG DEFER TRAINING	
CFG7	1: (Default) PEG Train immediately following xxRESETB de assertion 0: PEG Wait for BIOS for training



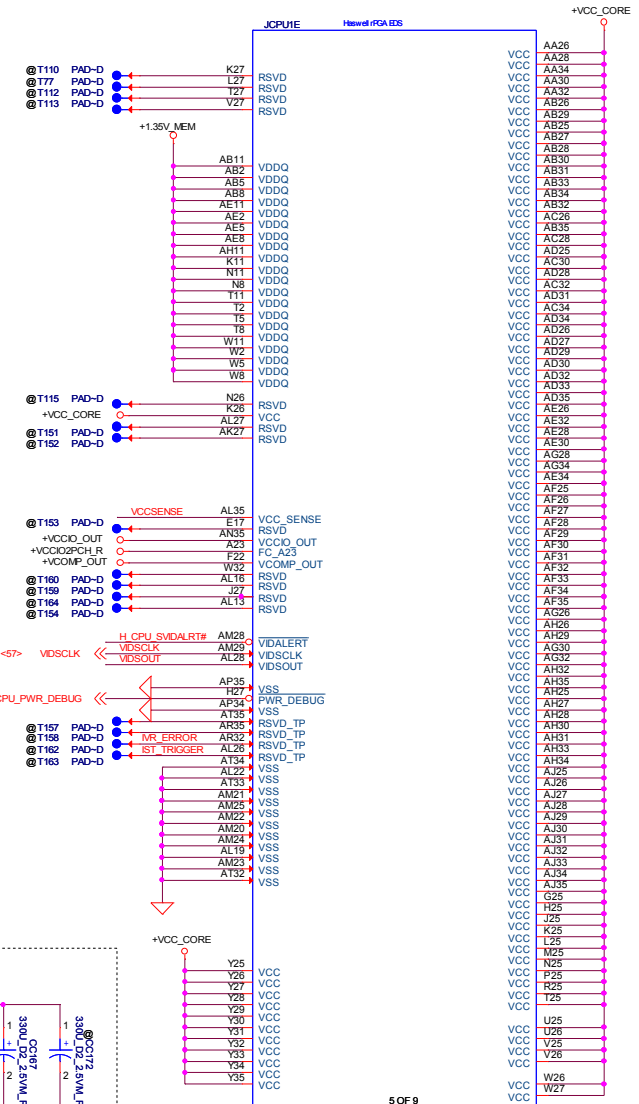
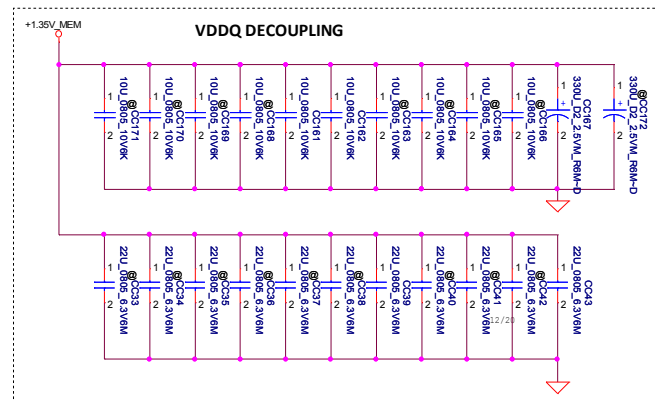
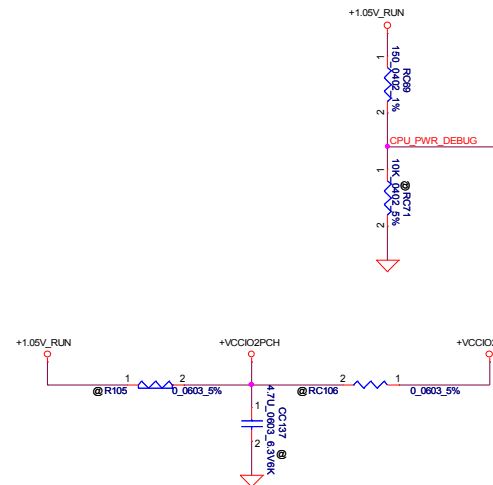
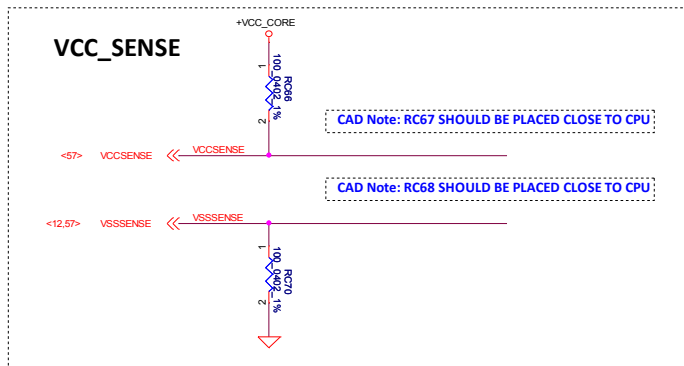
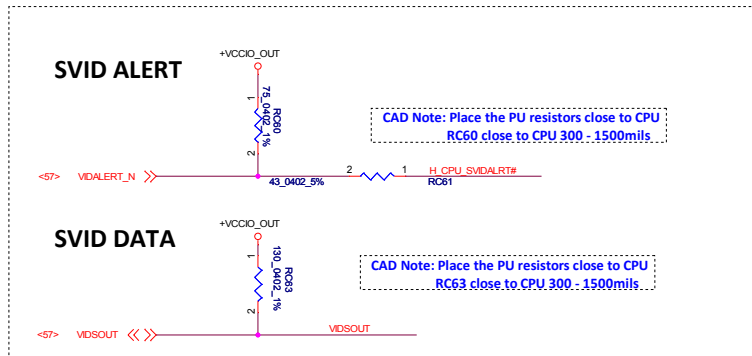
CPU socket Reverse type.



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CPU socket Reverse type.

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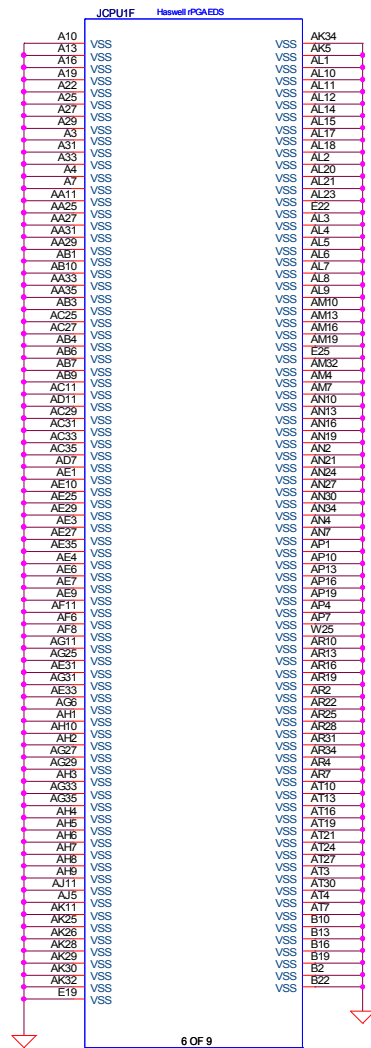
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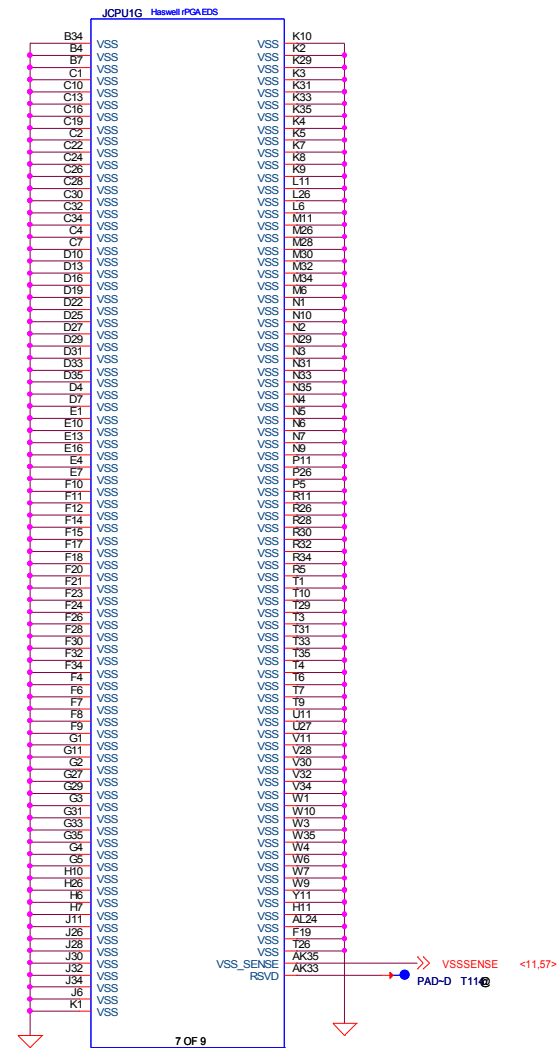
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CONN@

CPU socket Reverse type.



CONN@

CPU socket Reverse type.

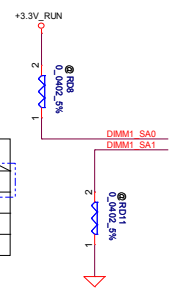
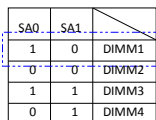
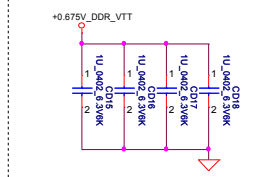
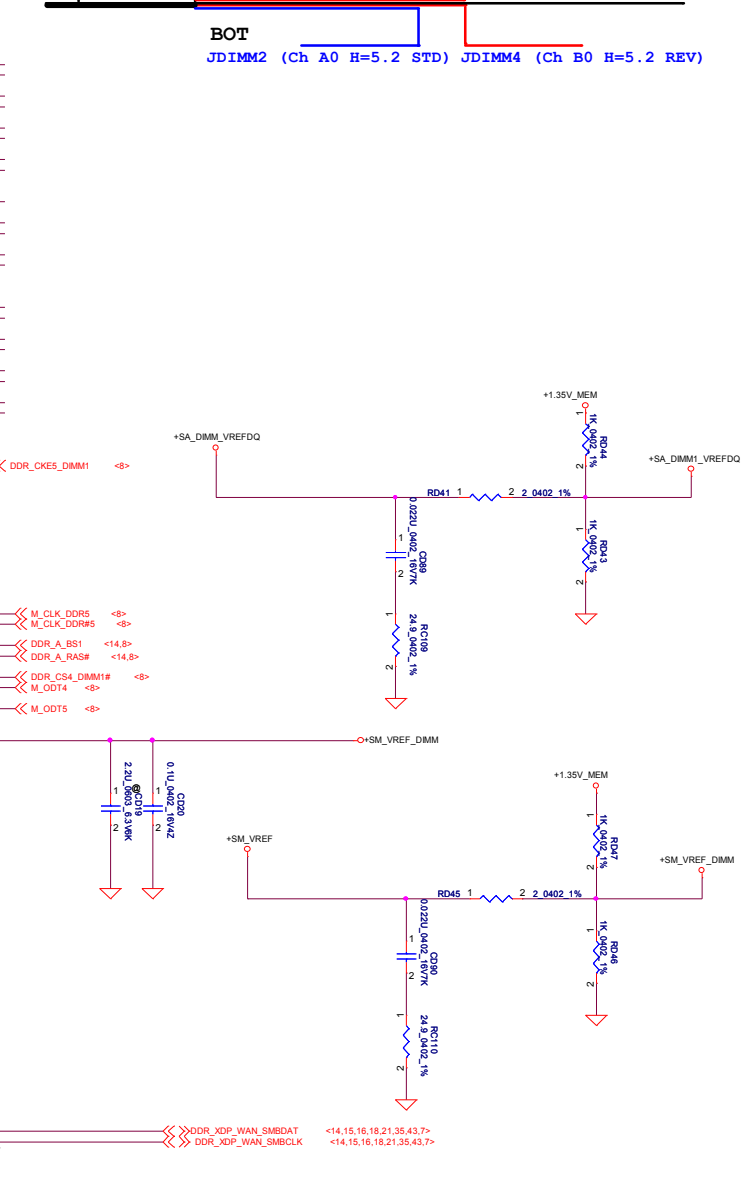
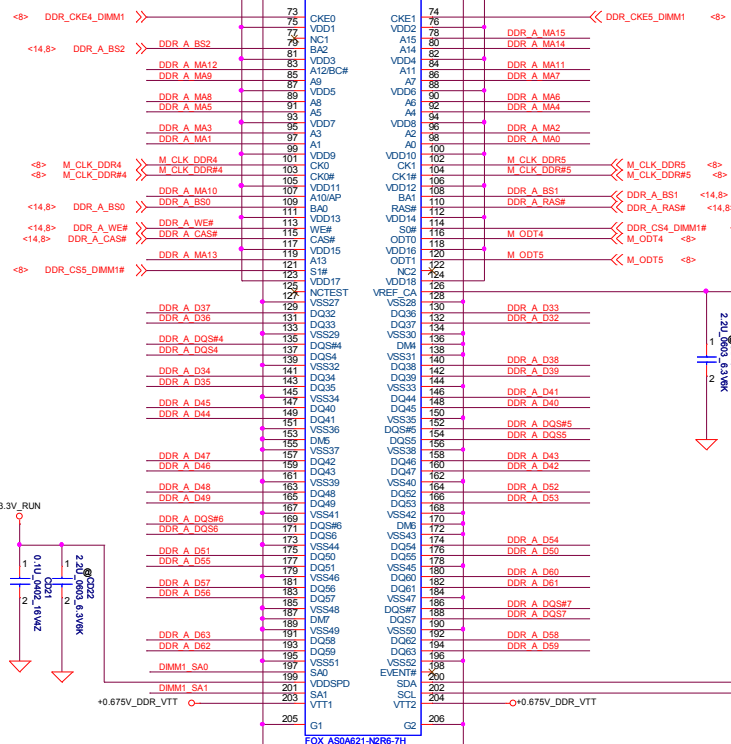
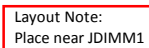
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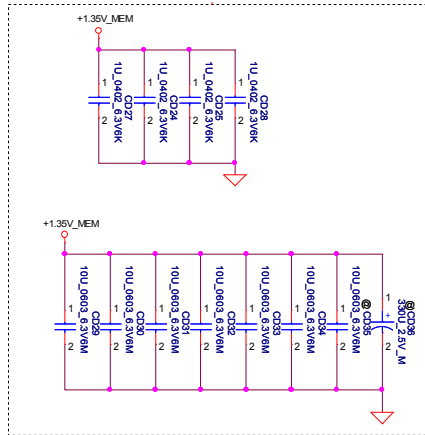


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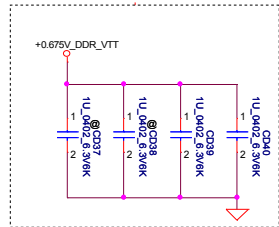


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 <13,8> DDR_A_DQ0..63 << >>
 <13,8> DDR_A_DQS#0..7 << >>
 <13,8> DDR_A_MA#0..15 << >>

Layout Note:
Place near JDIMM2

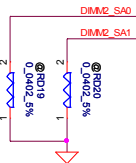


Layout Note:
Place near JDIMM2, Pin 203, 204

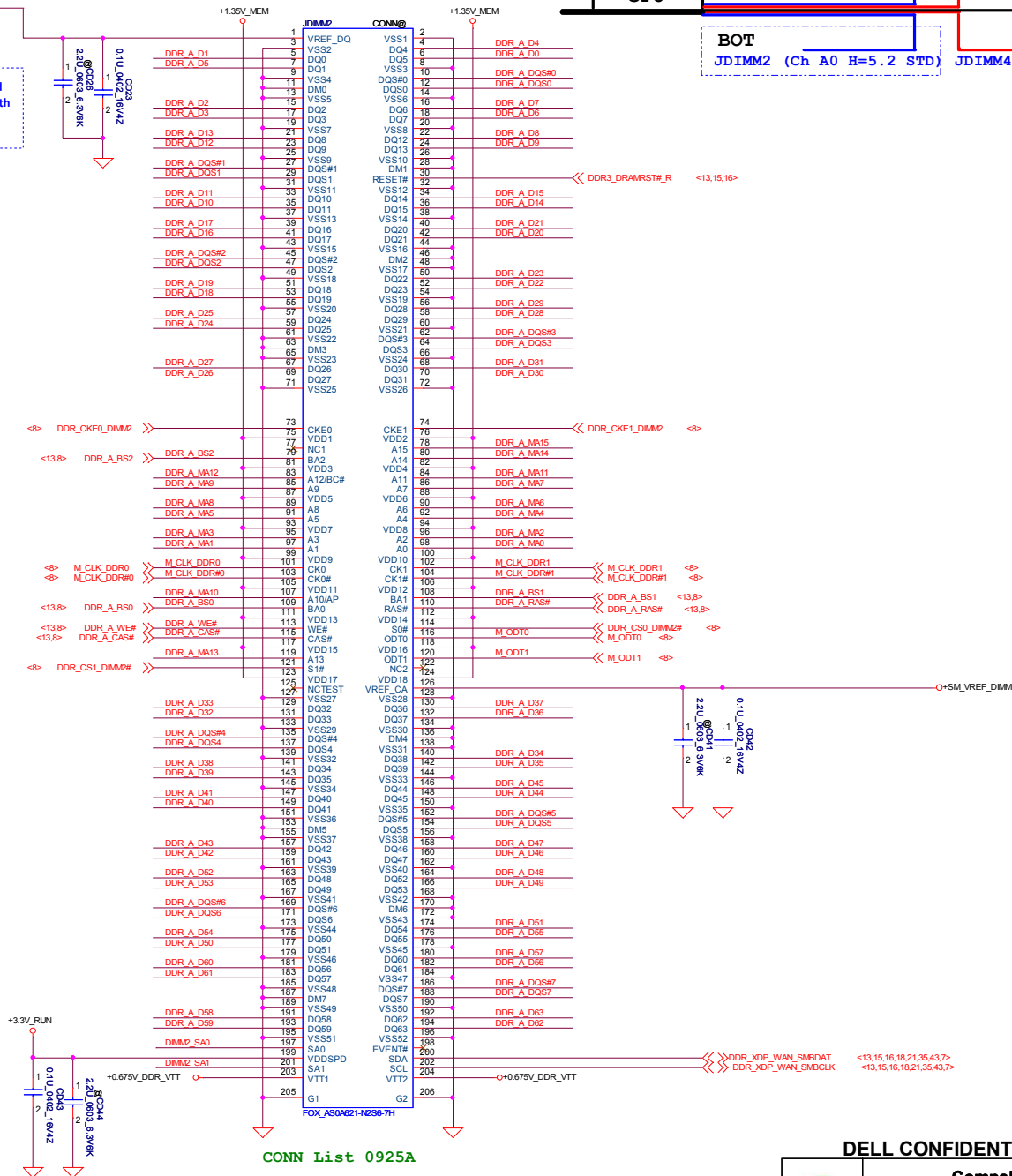


DIMM Select

SA0	SA1	
1	0	DIMM1
0	0	DIMM2
1	1	DIMM3
0	1	DIMM4



JDIMM2 STD Type H=5.2



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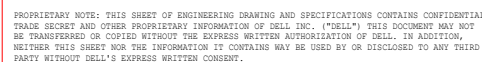
DDR3-SODIMM SLOT2

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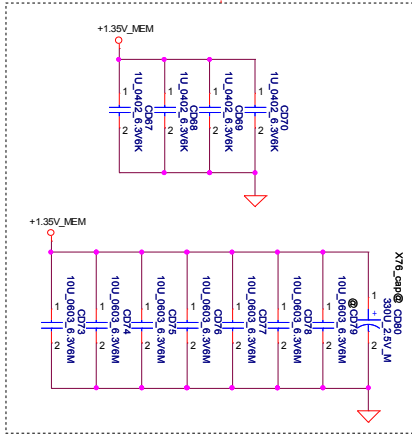


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<15,8> DDR_B_DQ0..63 <>>>
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<15,8> DDR_B_M#0..15 <>>>

JDIMM4 REV Type H=5.2

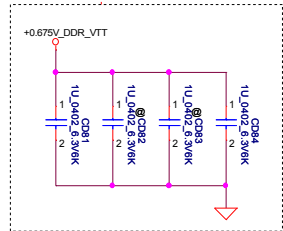
+SB_DIMM1_VREFDQ

Layout Note:
Place near JDIMM4



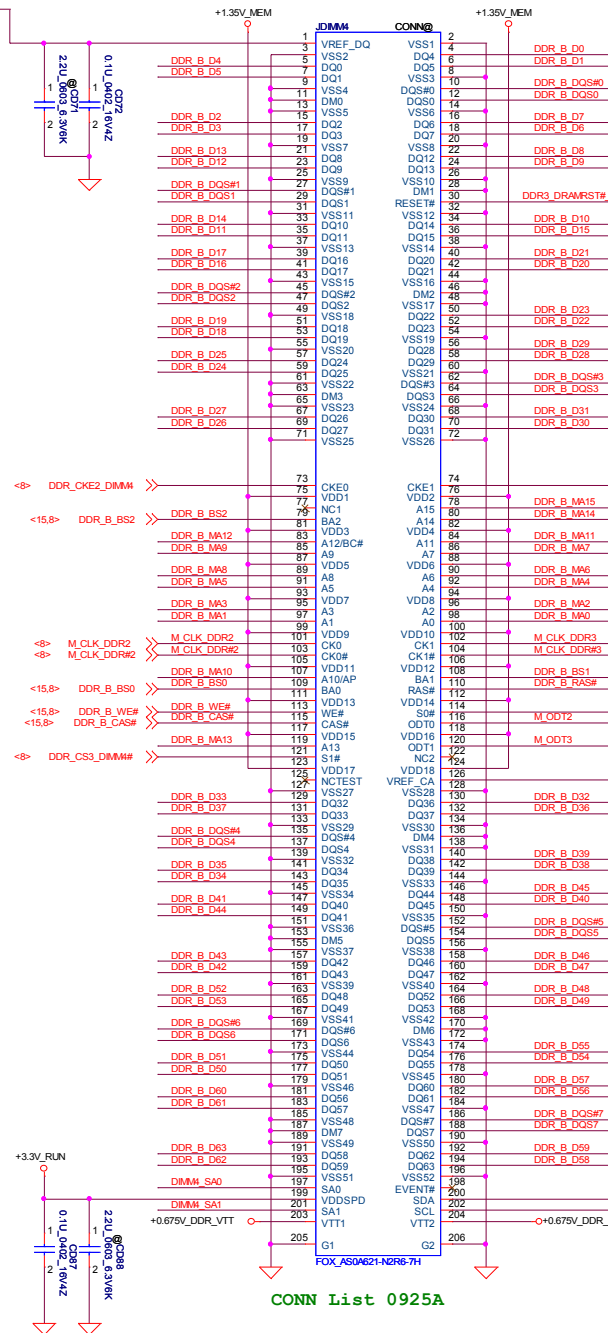
All VREF traces should
have 20 mil trace width
and 20 mil spacing to
other signals/planes.

Layout Note:
Place near JDIMM4.Pin 203,204



DIMM Select

SA0	SA1	
1	0	DIMM1
0	0	DIMM2
1	1	DIMM3
0	1	DIMM4



CONN List 0925A

JDIMM3 (Ch B1 H=9.2 REV)

JDIMM1 (Ch A1 H=5.2 REV)

CPU

TOP

BOT

JDIMM2 (Ch A0 H=5.2 STD)

JDIMM4 (Ch B0 H=5.2 REV)

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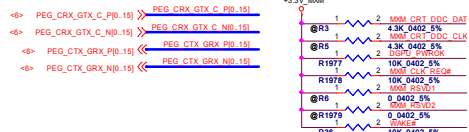
DDRIII-SODIMM SLOT4

LA-9772P

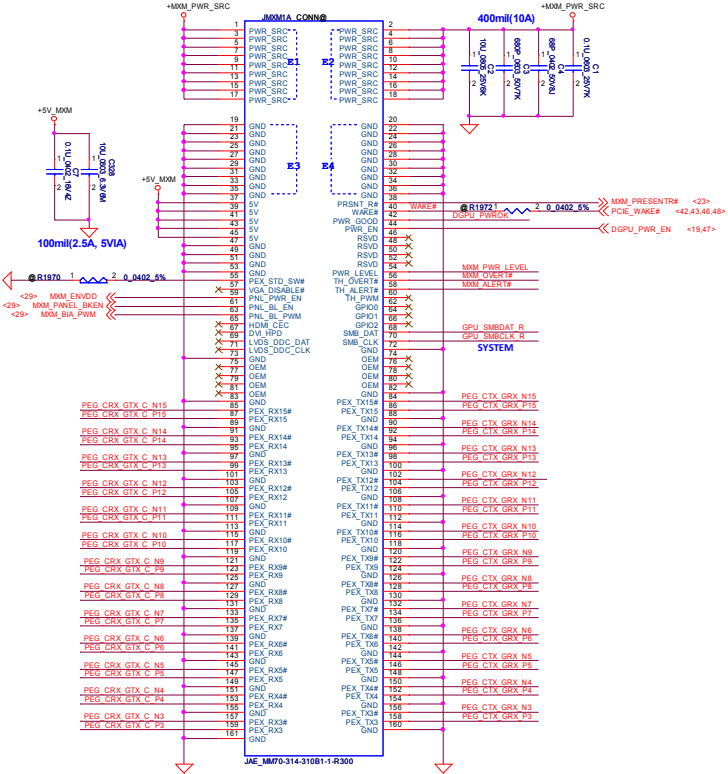
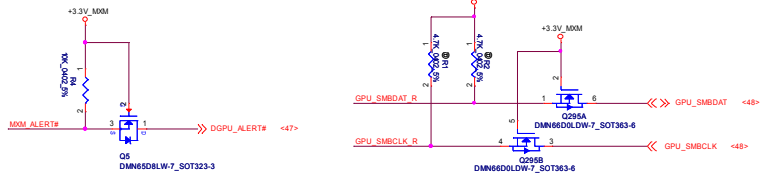
Date: Friday, April 28, 2014

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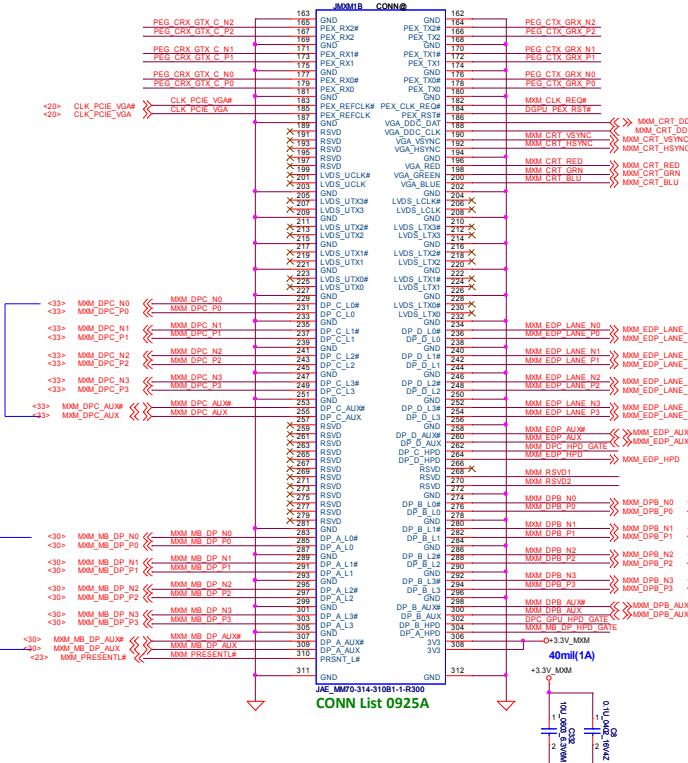


C2 keep 15" height limit.



HDMI/Docking DP MUX

MB DP



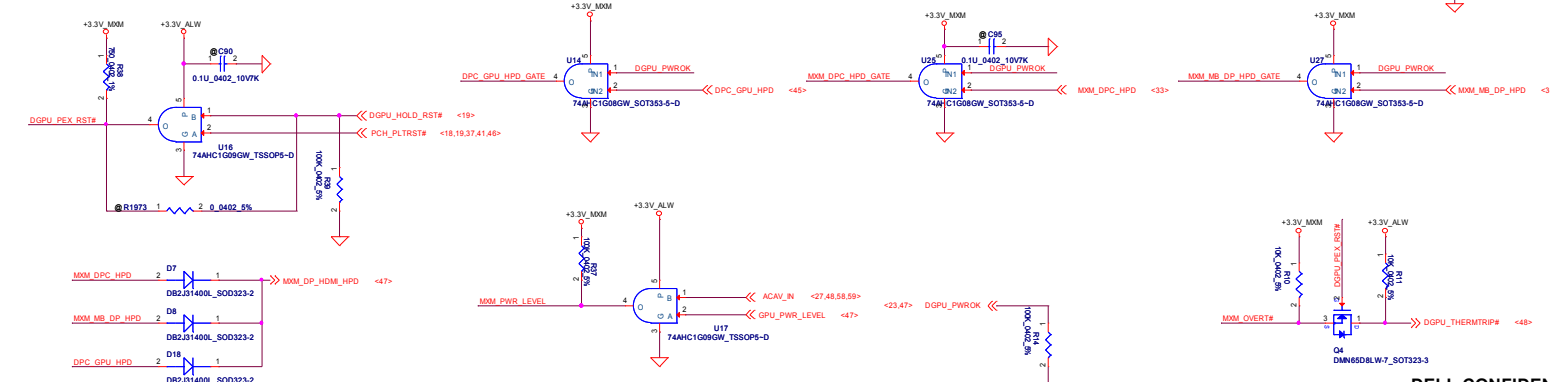
CRT

EDP

Docking DP port 2

CONN List 0925A

CONN List 0925A

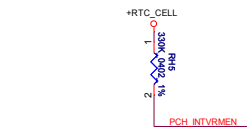


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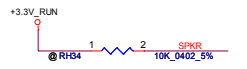


Compal Electronics, Inc.		
MXM		
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0.1	LA-9772P	0.1
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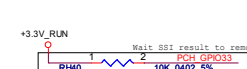


INTVRMEN - INTEGRATED SUS 1.05V VRM
ENABLE
High - Enable Internal VRs
Low - Enable External VRs



NO REBOOT STRAP
DISABLED WHEN LOW (DEFAULT)
ENABLED WHEN HIGH

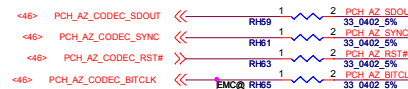
FLASH DESCRIPTOR SECURITY OVERRIDE
LOW = DISABLED (DEFAULT)
HIGH = ENABLED



CMOS_CLR1	CMOS setting
Shunt	Clear CMOS
Open	Keep CMOS

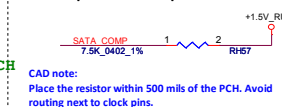
ME_CLR1	TPM setting
Shunt	Clear ME RTC Registers
Open	Keep ME RTC Registers

HDA for Codec



1/16 UH1 change PN to SA00006P30L IC A31 DH82QM87 QE98 C1 FCBGA 695P PCH

SATA Impedance Compensation



CAD note:
Place the resistor within 500 mils of the PCH. Avoid routing next to clock pins.

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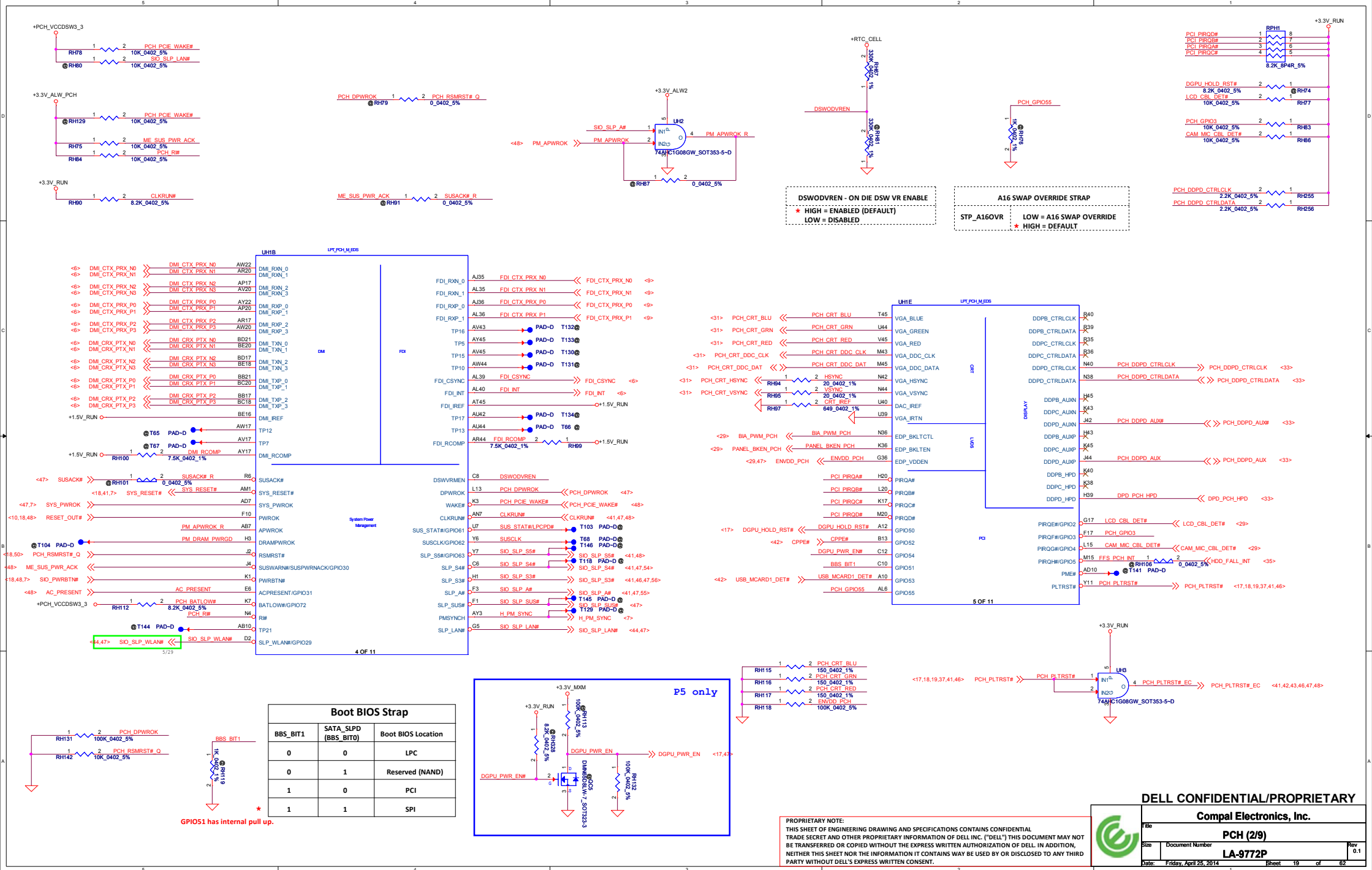
Compal Electronics, Inc.

PCH (1/9)

LA-9772P

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Date: Friday, April 25, 2014 Sheet 18 of 62

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Title	BOH (210)
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	PCH (2/9)
Size	Document Number

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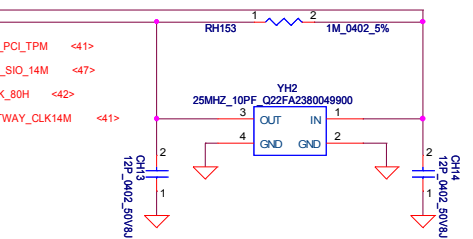
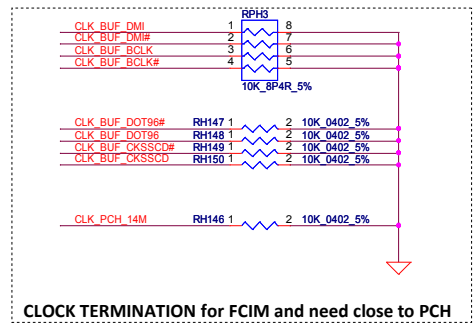
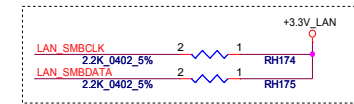
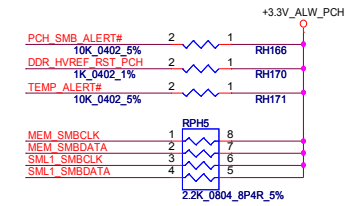
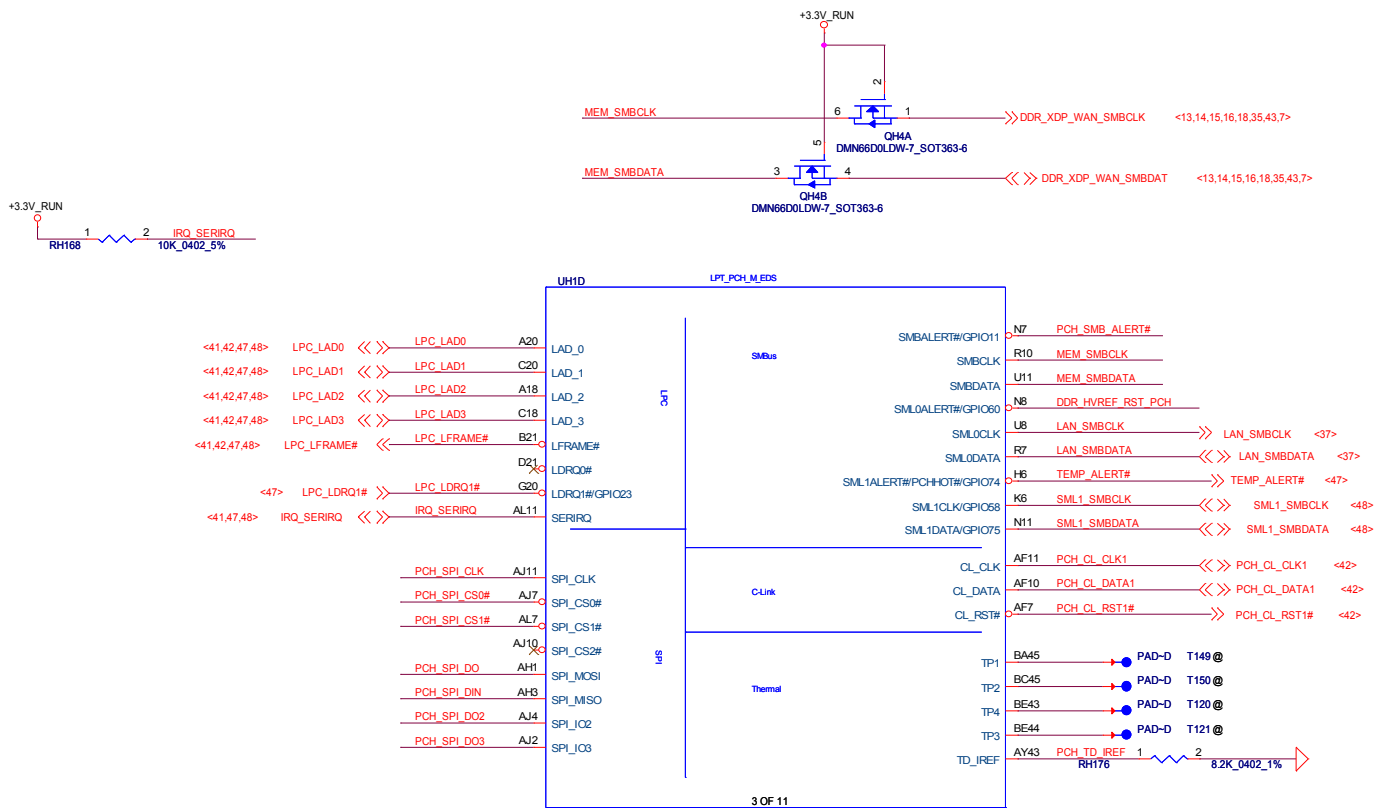
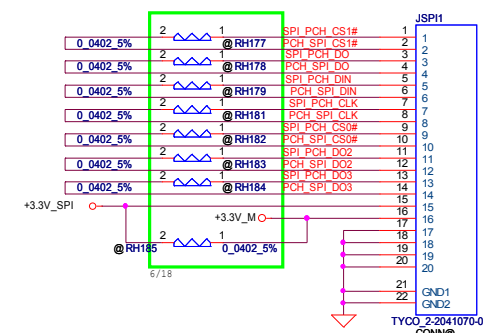
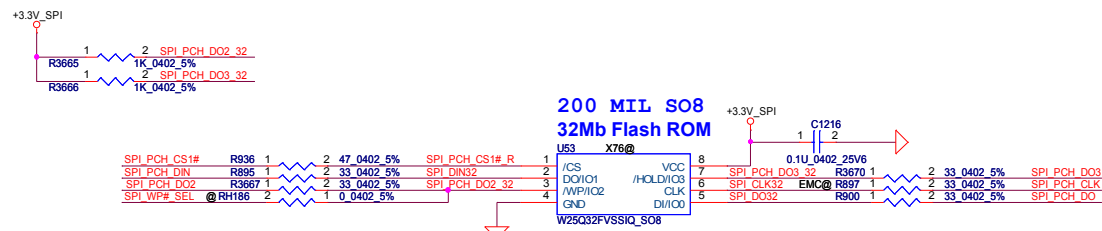
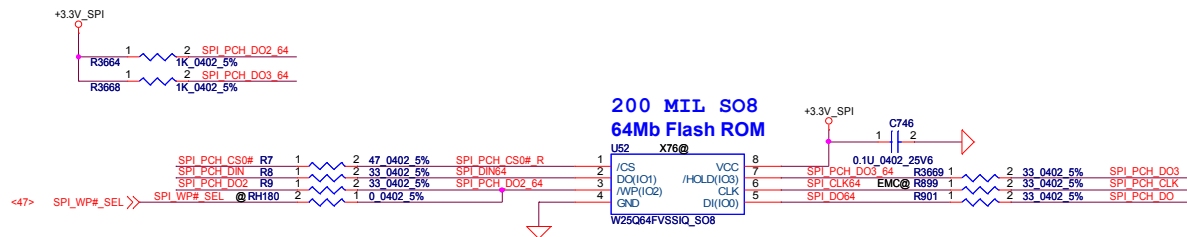
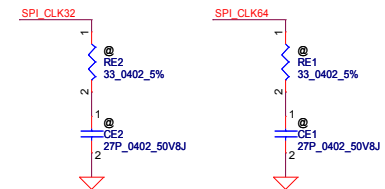


Figure 10 shows seven termination circuit diagrams for the 1000BASE-T PHY. Each diagram represents a different signal line and its termination configuration:

- CLK_PCI_5048:** Signal line with a 100-ohm termination resistor connected to a 50V reference voltage. The signal line is labeled with pin 1 and 2, and the resistor is labeled 100Ω and 50V/Ω.
- CLK_PCI_MEC:** Signal line with a 100-ohm termination resistor connected to a 50V reference voltage. The signal line is labeled with pin 1 and 2, and the resistor is labeled 100Ω and 50V/Ω.
- CLK_PCI_DOCK:** Signal line with a 100-ohm termination resistor connected to a 50V reference voltage. The signal line is labeled with pin 1 and 2, and the resistor is labeled 100Ω and 50V/Ω.
- CLK_PCI_LOOPBACK:** Signal line with a 100-ohm termination resistor connected to a 50V reference voltage. The signal line is labeled with pin 1 and 2, and the resistor is labeled 100Ω and 50V/Ω.
- CLK_PCI_TPM:** Signal line with a 100-ohm termination resistor connected to a 50V reference voltage. The signal line is labeled with pin 1 and 2, and the resistor is labeled 100Ω and 50V/Ω.
- CLK_SIO_14M:** Signal line with a 100-ohm termination resistor connected to a 50V reference voltage. The signal line is labeled with pin 1 and 2, and the resistor is labeled 100Ω and 50V/Ω.
- JETWAY_CLK14M:** Signal line with a 100-ohm termination resistor connected to a 50V reference voltage. The signal line is labeled with pin 1 and 2, and the resistor is labeled 100Ω and 50V/Ω.



if support 1MHz, need change to 499ohm+/-5%



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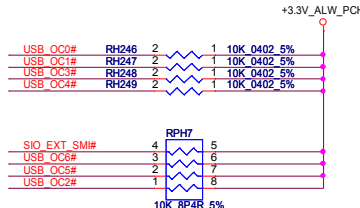
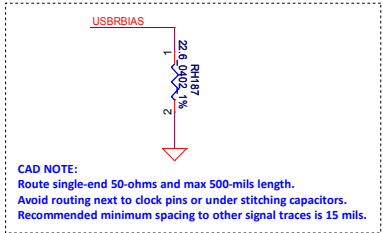
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Fixed Signals				Muxed Signals		Fixed Signals						Muxed Signals		Fixed Signals			
USB3_1	USB3_2	USB3_5	USB3_6	PCIE_1	PCIE_2	PCIE_3	PCIE_4	PCIE_5	PCIE_6	PCIE_7	PCIE_8	SATA_4	SATA_5	SATA_0	SATA_1	SATA_2	SATA_3
				(00)	(00)							(00)	(00)				
				USB3_3	USB3_4							PCIE_1	PCIE_2				
				(01)	(01)							(01)	(01)				

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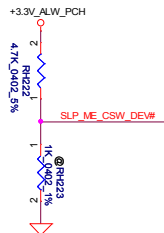
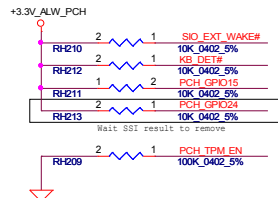
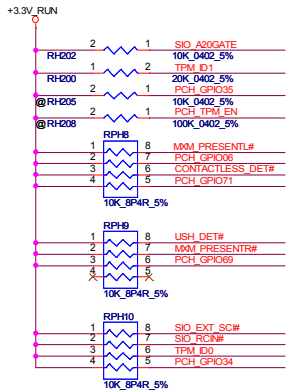
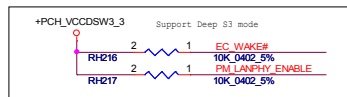
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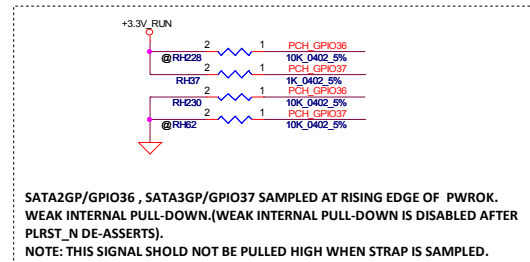
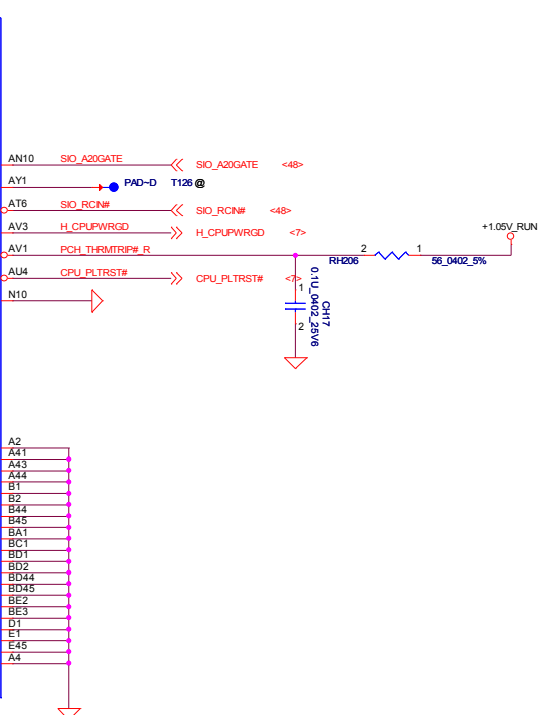
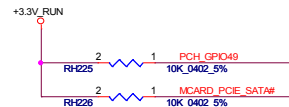
Date: Friday, April 25, 2014

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Rev 0.1



PLL ON DIE VR ENABLE
 * ENABLED - HIGH(DEFAULT)
 DISABLED - LOW



Note: GPIO strap option is only available for SATA/PCIE muxed signals to support mSATA/mini PCIE port switching

GPIO16	GPIO49
0: PCIE1	0: PCIE2
1: SATA4	1: SATA5

00b or 01b: Assign muxed signal to desired port
 10b: Reserved
 11b: Assign desired port based on GPIO

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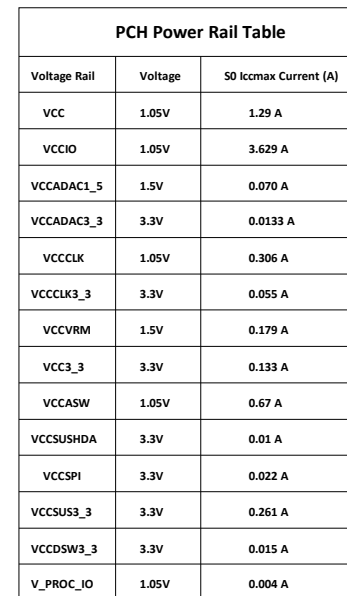
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PCH (6/9)

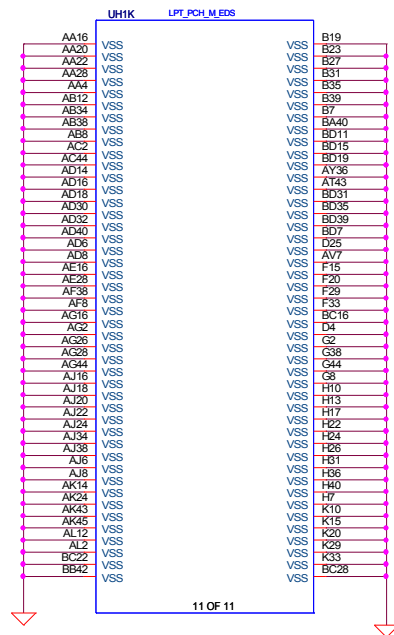
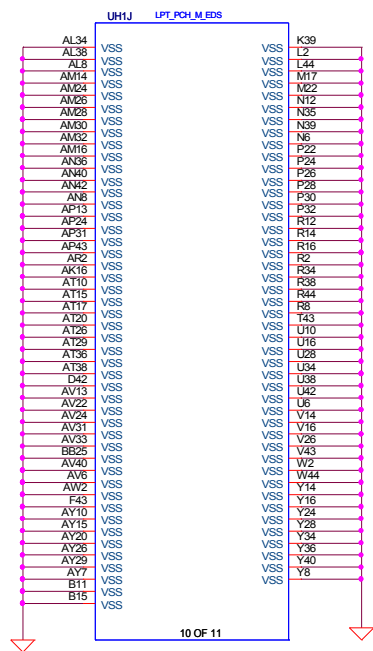
LA-9772P

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Title			
PCH (7/9)			
Size	Document Number	Rev	
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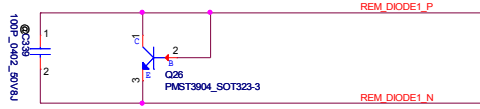


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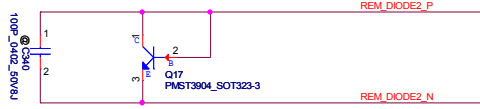
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Size	Document Number	LA-9772P	
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		Rev	0.1

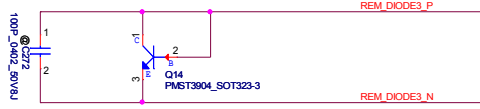
Place Q26 under CPU
Place C339 close to the Q26



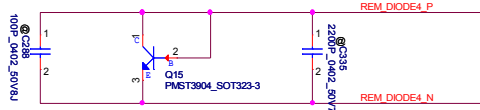
DP2/DN2 for SODIMM on Q17(TOP),
place Q17 close to SODIMM and C340 close to Q2



DP3/DN3 for Butterfly CHA on Q14(BOT),
place Q14 close to Butterfly CHA and C272 close to Q14

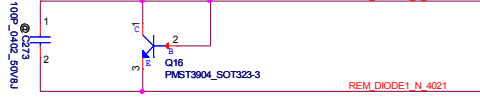


DP4/DN4 for Skin on Q15,
place Q15 close to Vcore VR choke and C288 close to Q15

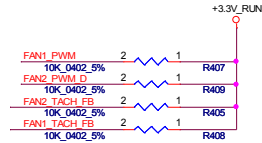
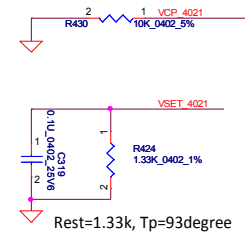
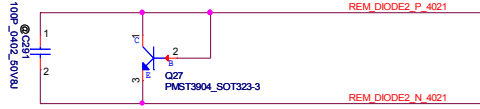


REM_DIODE1_N <>> REM_DIODE1_P <>>
REM_DIODE1_P <>> REM_DIODE2_P <>>
REM_DIODE2_P <>> REM_DIODE2_N <>>
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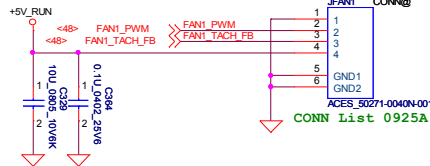
Place Q16 under MXM(TOP side)
Place C273 close to the Q16



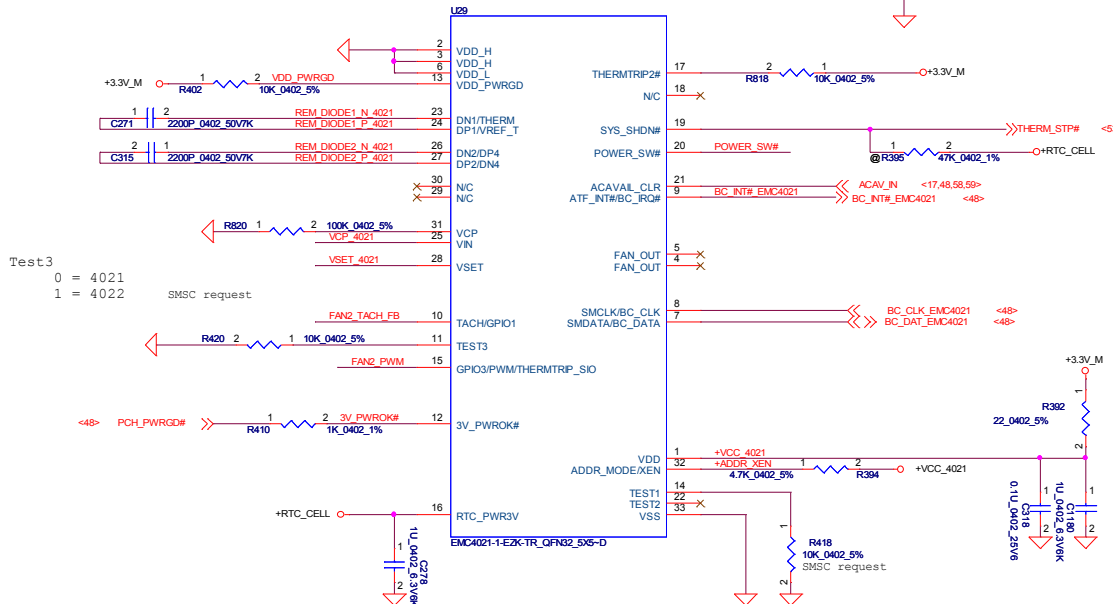
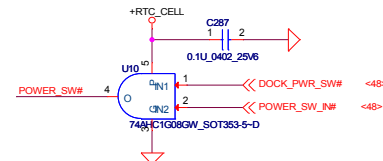
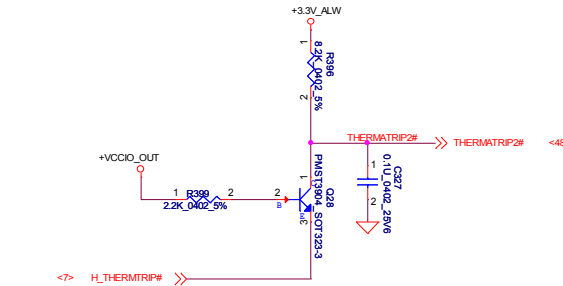
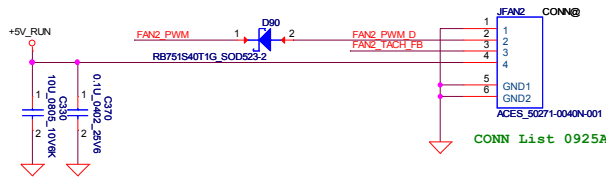
DP2/DN2 for MXM on Q27(BOT side),
place Q27 close to Butterfly CHB and C291 close to Q27



CPU FAN



MXM FAN



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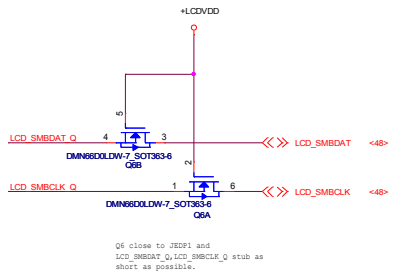
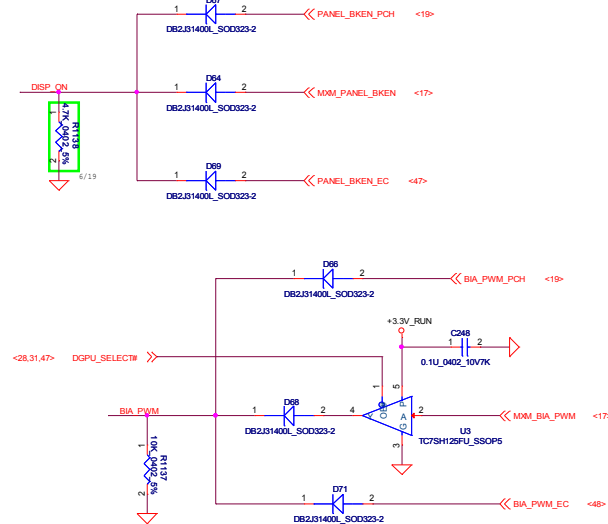
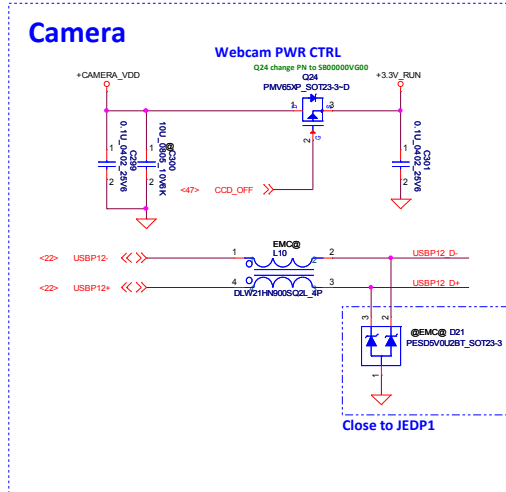
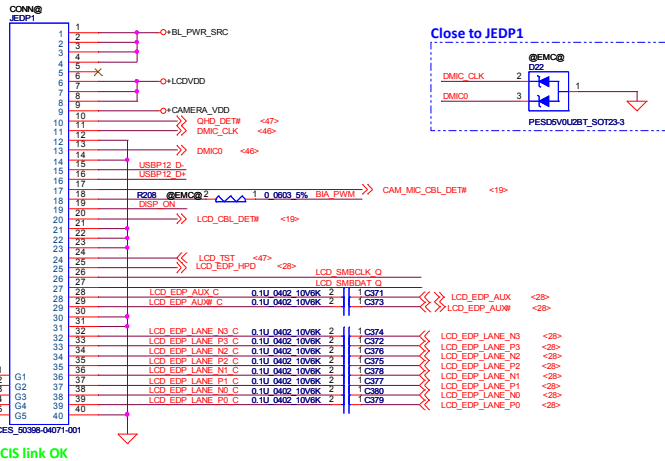
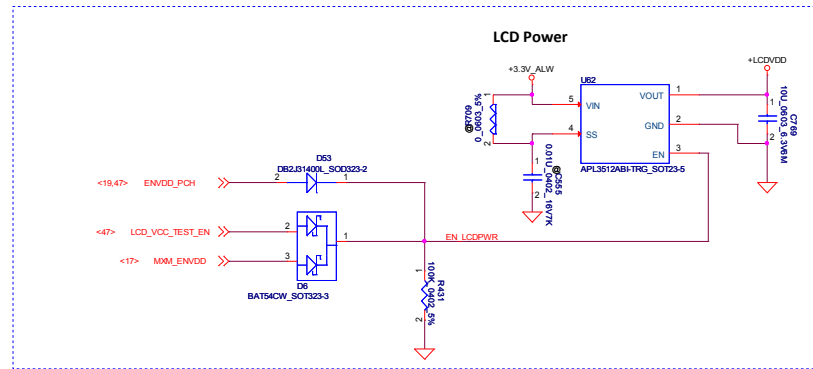
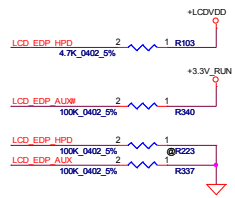
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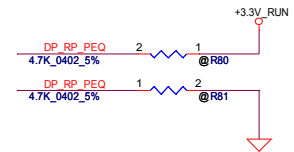
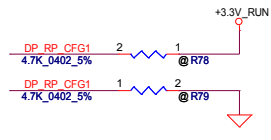
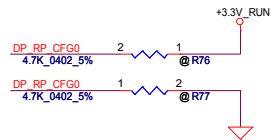
FAN control

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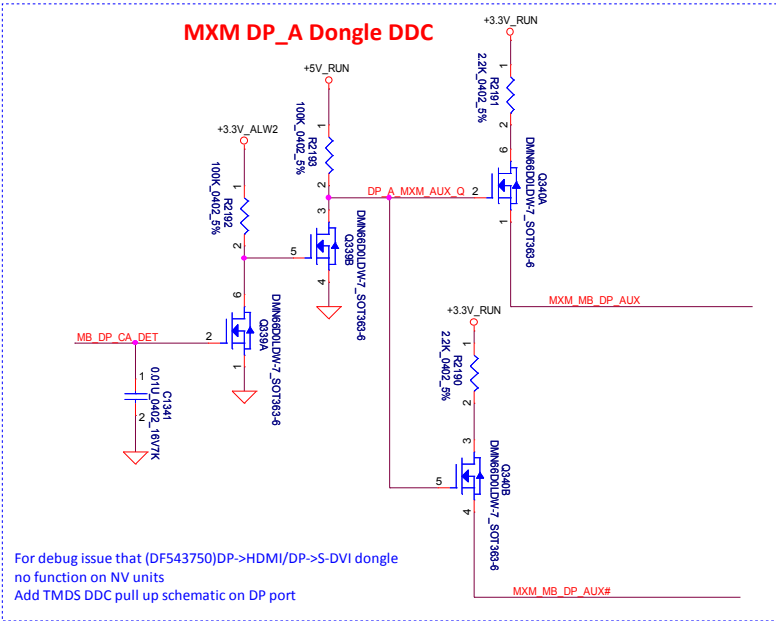
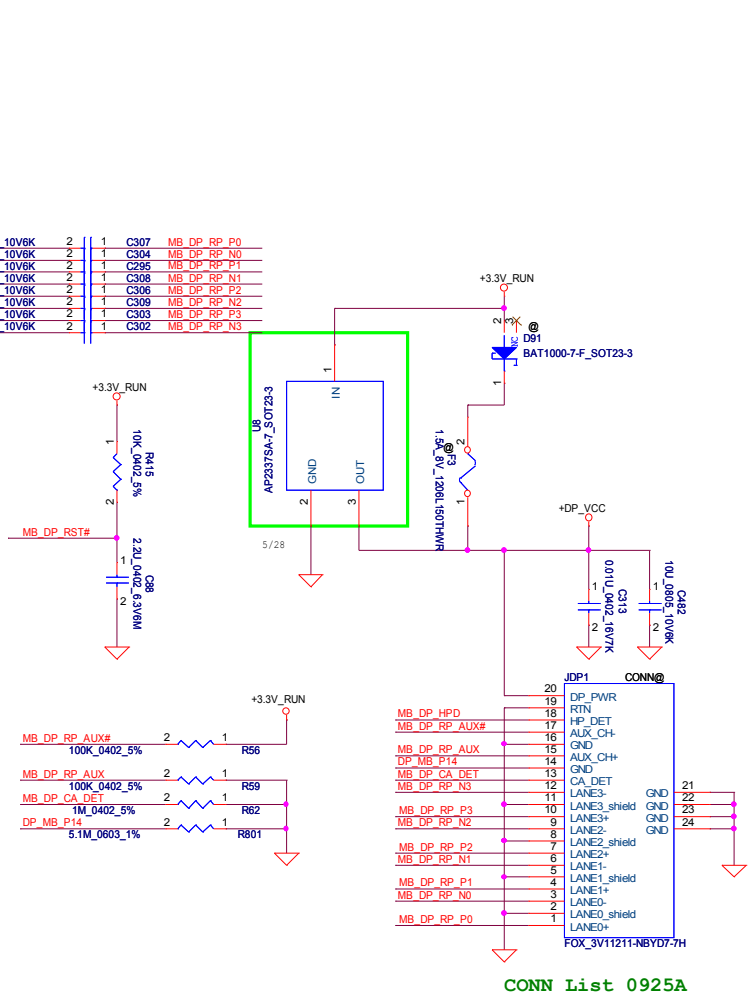
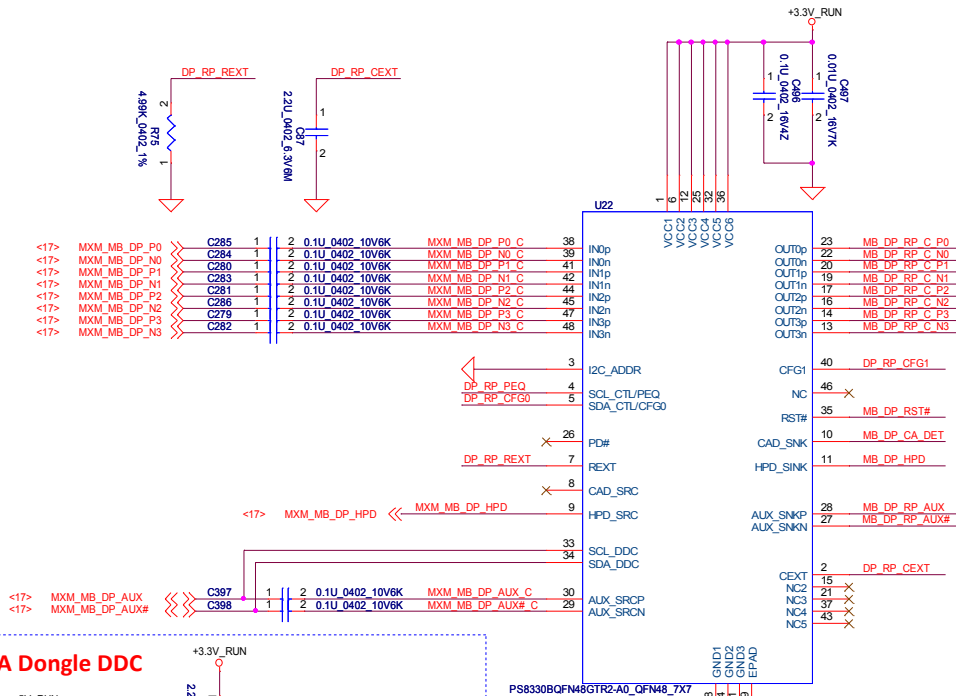




Configuration pin for automatic EQ and AUX interception; Internal pull down at ~150kΩ, 3.3V I/O.
 L: default, automatic EQ enable & AUX interception enable
 H: automatic EQ disable & AUX interception enable
 M: automatic EQ disable & AUX interception disable, no pre-emphasis, 600mVpp swing

Configuration pin for auto test and input offset cancellation, 3.3V IO, internal pull up at ~150K
 H: default, auto test disable & input offset cancellation enable
 L: auto test enable & input offset cancellation enable
 M: auto test disable & input offset cancellation disable

Programmable input equalization levels; Internal pull down at ~150kΩ, 3.3V I/O.
 L: default, LEQ, compensate channel loss up to 12dB @ HBR2
 H: HEQ, compensate channel loss up to 15dB @ HBR2
 M: LLEQ, compensate channel loss up to 5dB @ HBR2



For debug issue that (DF543750)DP->HDMI/DP->S-DVI dongle no function on NV units
 Add TMD5 DDC pull up schematic on DP port

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		Compal Electronics, Inc.	
		DP Conn	
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	CRT_SWITCH	DGPU_SELECT#	EDID_SELECT#	Output
DSC mode output to MB VGA	0	0	0	SDAA to SDA1 SCLA to SCL1 REDA to RED1 GRNA to GRN1 BLUA to BLU1 SHA to SH1 SVA to SV1
DSC mode output to docking VGA	1	0	0	SDAA to SDA2 SCLA to SCL2 REDA to RED2 GRNA to GRN2 BLUA to BLU2 SHA to SH2 SVA to SV2
UMA mode output to MB VGA	0	1	1	SDAB to SDA1 SCLB to SCL1 REDB to RED1 GRNB to GRN1 BLUB to BLU1 SHB to SH1 SVB to SV1
UMA mode output to docking VGA	1	1	1	SDAB to SDA2 SCLB to SCL2 REDB to RED2 GRNB to GRN2 BLUB to BLU2 SHB to SH2 SVB to SV2



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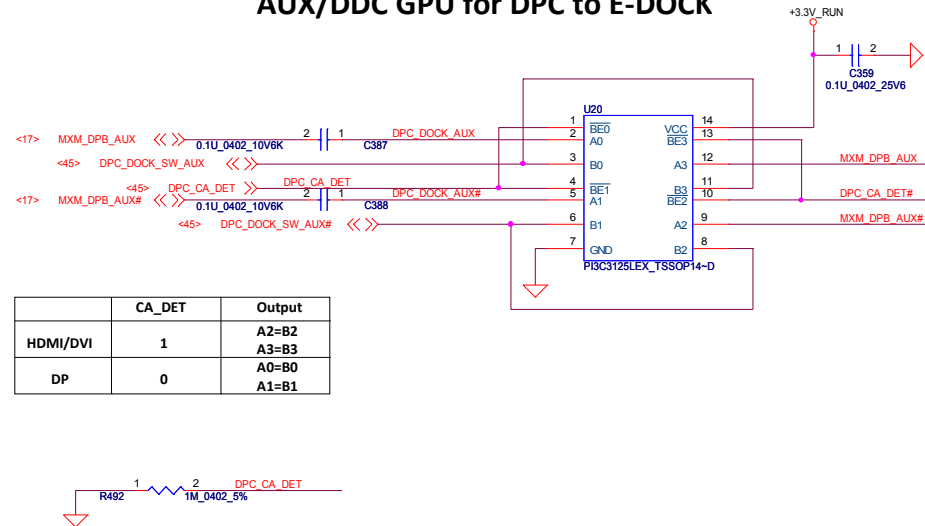
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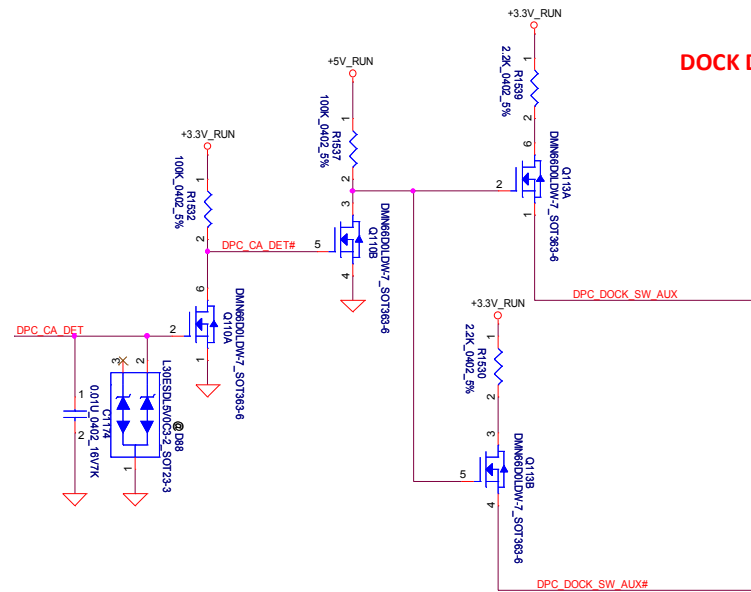
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Size	Document Number	Rev	
	LA-9772P	0.1	
Date:	Friday, April 25, 2014	Sheet	31 of 62

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AUX/DDC GPU for DPC to E-DOCK



DOCK DPB(PORT2) DDC



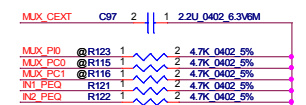
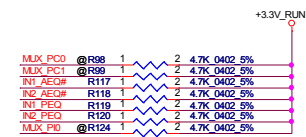
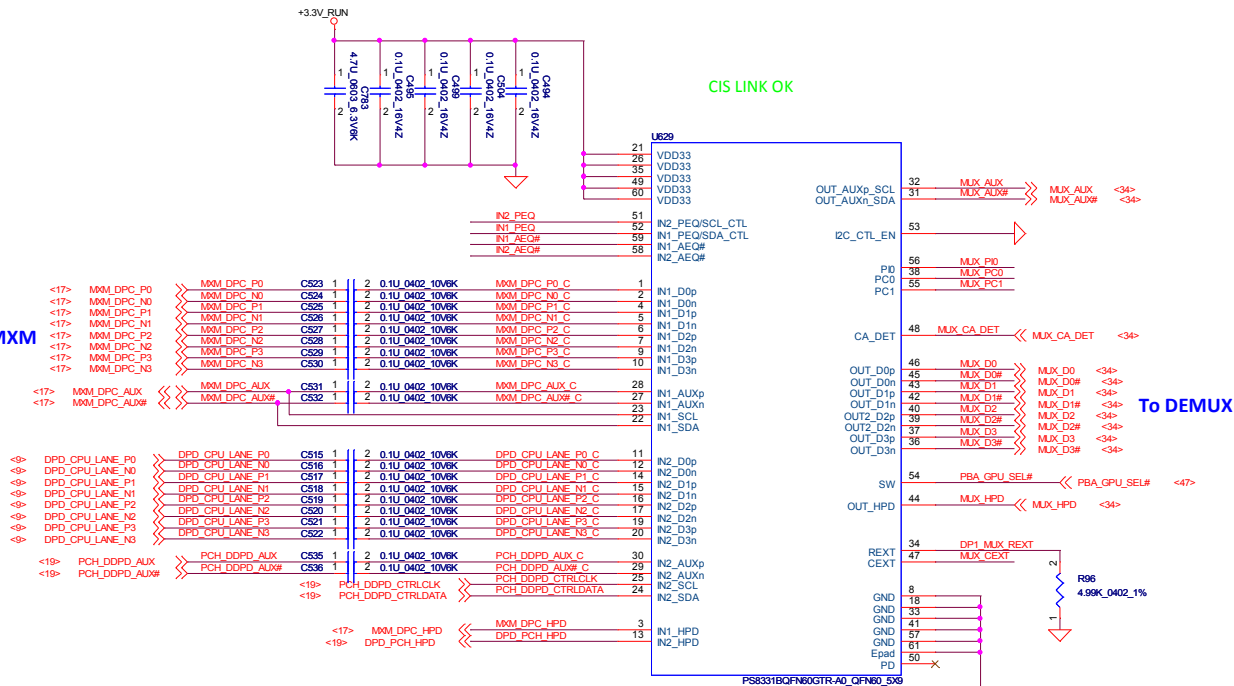
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Document Number		0.1	
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SW	Channel	Source
0(default)	DO=IN1	MMX
1	DO=IN2	CPU

INy_PEQ(y=1,2)
 L: default, LEQ, compensate channel loss up to 11.5dB @HBR2
 H: HEQ, compensate channel loss up to 14.5dB @HBR2
 M: LEQ, compensate channel loss up to 8.5dB @HBR2

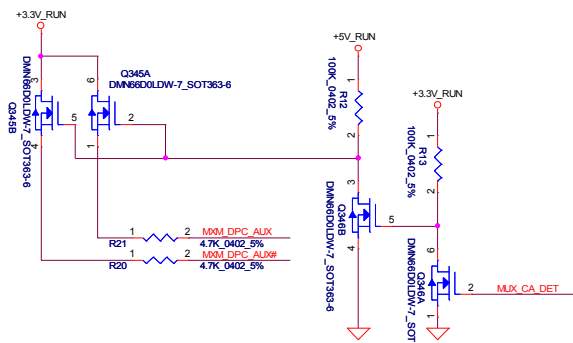
INy_AEQ#(y=1,2)
 L: Automatic EQ enable (default)
 H: Automatic EQ disable

PIO
 L: Auto test disable & input offset cancellation enable (default)
 H: Auto test enable & input offset cancellation enable
 M: Auto test disable & input offset cancellation disable

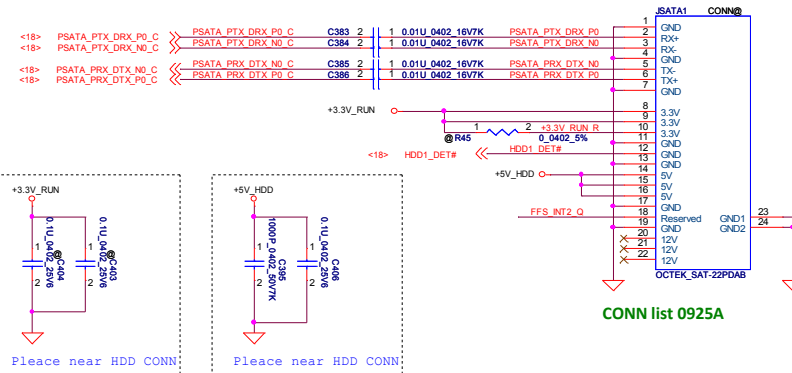
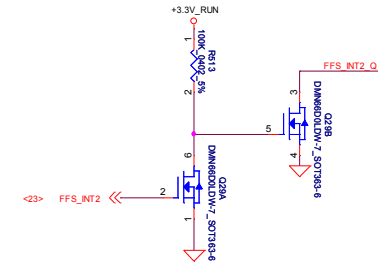
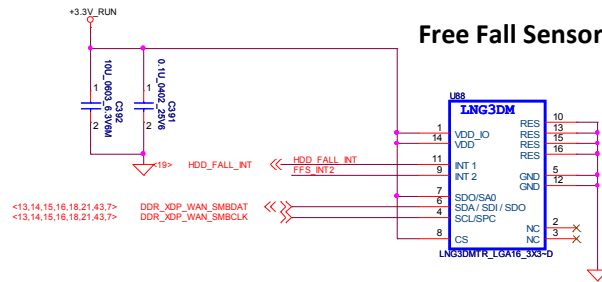
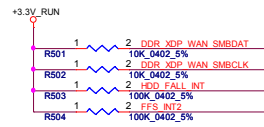
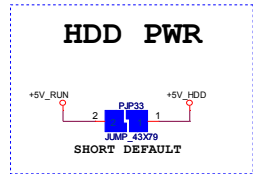
PC0
 L: AUX interception enable, driver configuration is set by link training (default)
 H: AUX interception disable, driver output with fixed 800mV and 0dB
 M: AUX interception disable, driver output with fixed 400mV and 0dB

PC1
 L: default
 H: Output swing +20%
 M: Output swing -16.7%

DOCK DPA(PORT1) DDC & HDMI DDC-before PS8331



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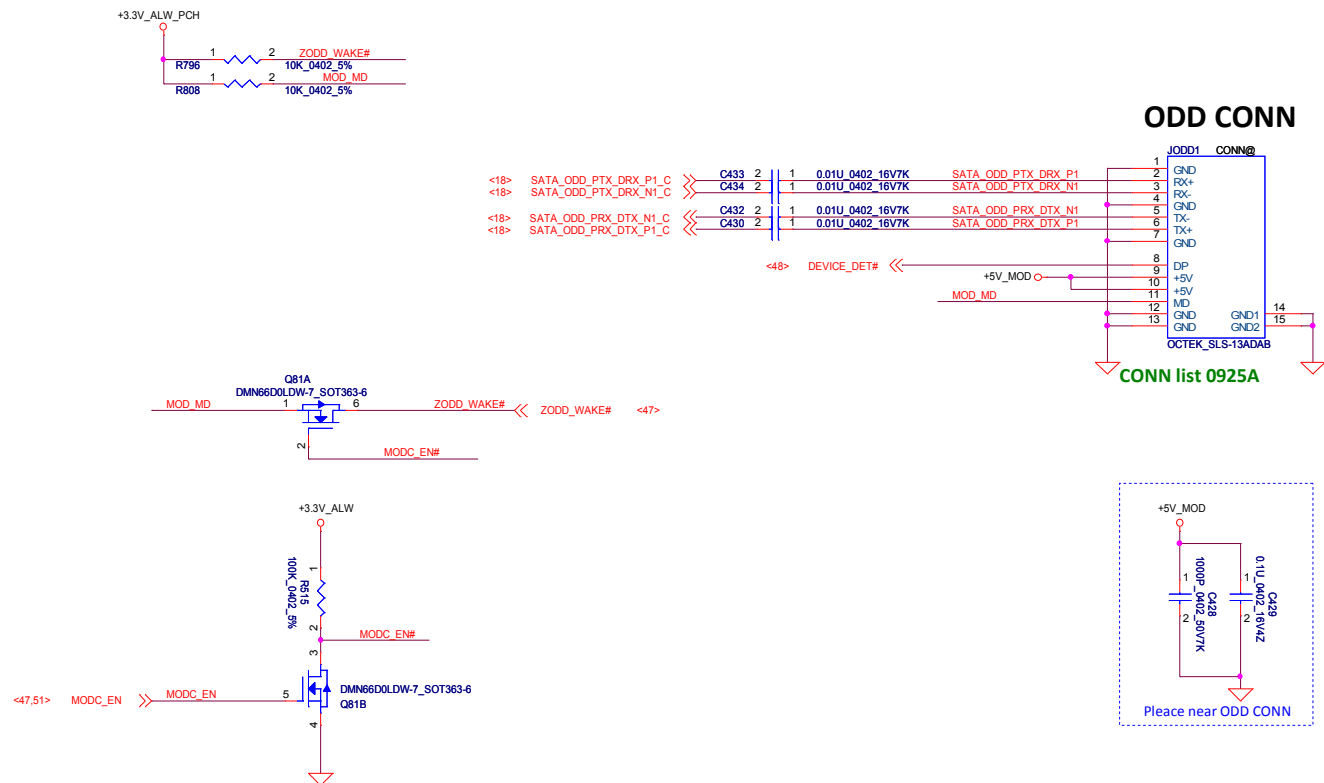
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HDD CONN

Size Document Number LA-9772P Rev 0.1

Date: Friday, April 25, 2014 Sheet 35 of 62

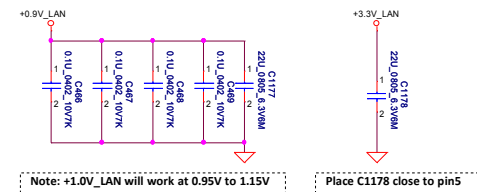
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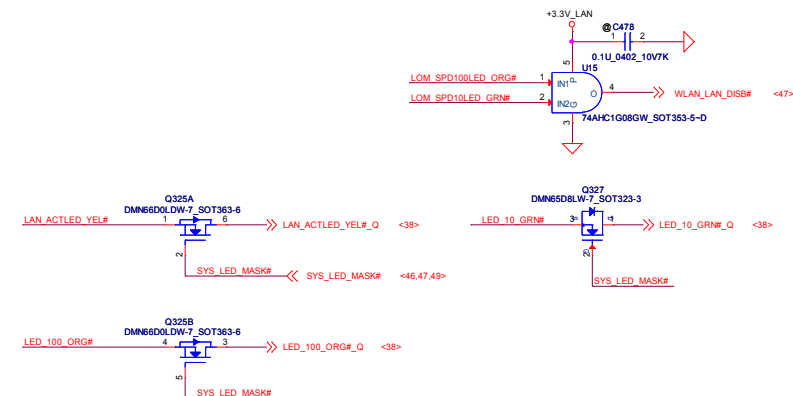
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Title			
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Size	Document Number	Rev	
		0.1	
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+0.9V_LAN POWER OPTIONS	
Shared with PCH 1.05V SVR	* Internal SRV
STUFF: R548 NO STUFF: L29	STUFF: L29 NO STUFF: R548



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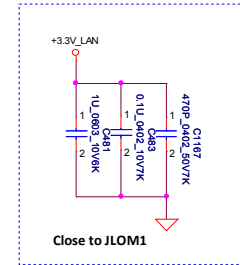
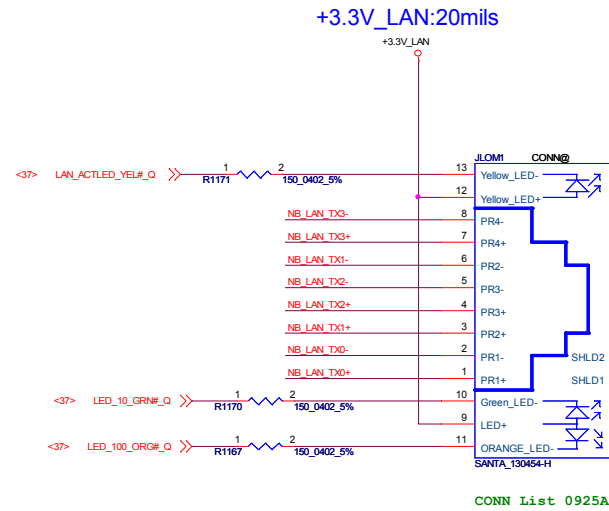
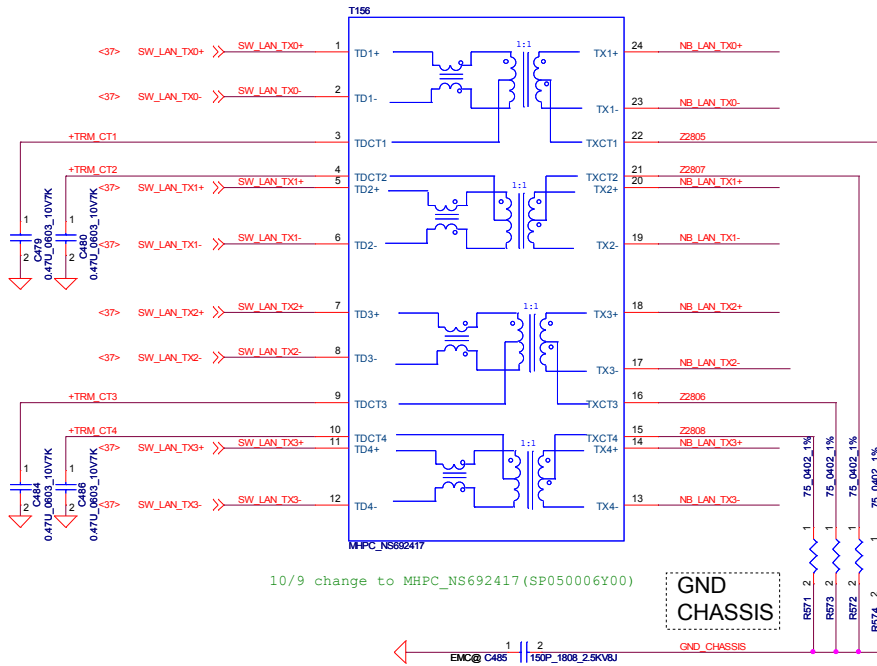
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LAN/LAN SW

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RJ45

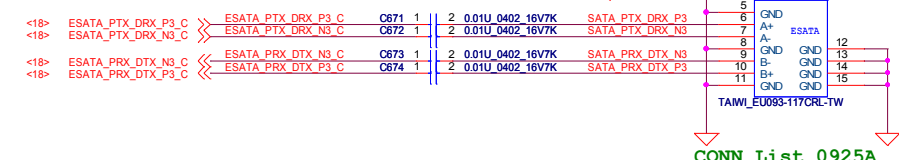
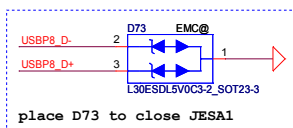
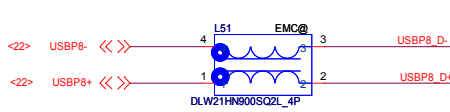
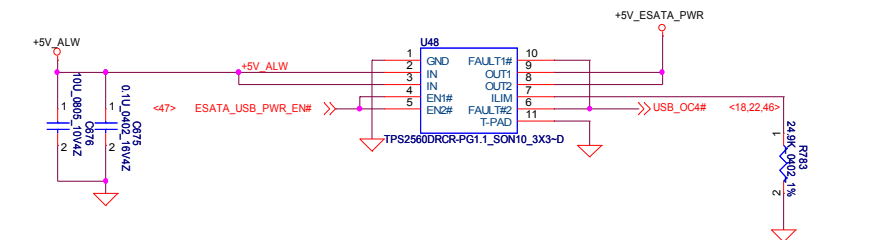
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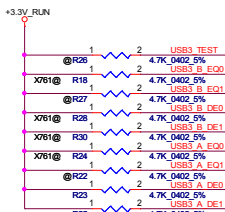
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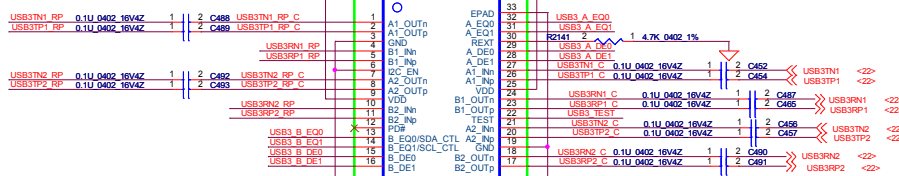
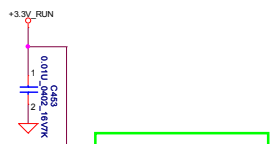


EQ: Equalizer control and program.
3.3V tolerant. Internally pulled down at ~150K ohm
[A_EQ1, A_EQ0] = [B_EQ1, B_EQ0]
LL: program EQ for channel loss up to 9.5dB
HL: program EQ for channel loss up to 13dB
HL: program EQ for channel loss up to 4.5dB
HL: program EQ for channel loss up to 7.5dB

TEST: Chip test mode enable.
3.3V tolerant. Internally pulled down at ~150K ohm.
L: Normal operation (default)
H: Test mode enable
for compliance test, this pin should be pulled to high.

DE: Programmable output pre-emphasis level setting.
3.3V tolerant. Internally pulled down at ~150K ohm
[A_DE1, A_DE0] = [B_DE1, B_DE0]
LL: 3.5dB de-emphasis
LH: No de-emphasis
HL: 2.5dB de-emphasis
HH: 5dB de-emphasis

Pin13: B_EQ0 / SDA_CTL Pin28: A_DE1 / NC
Pin14: B_EQ1 / SCL_CTL Pin29: A_DE0 / NC
Pin15: B_DE0 / QC_ADDR0 Pin31: A_EQ1 / NC
Pin16: B_DE1 / QC_ADDR1 Pin32: A_EQ0 / NC

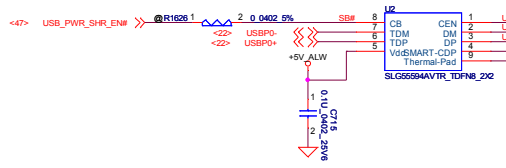


USB3.0 Redriver Select Component

	X76(Main) X7650931L01 PS8723B SA000064P10	X76(2nd) X7650931L02 PTN36242LBS SA000060K0L
U638	V	V
R18	V	
R28	V	
R30	V	
R24	V	

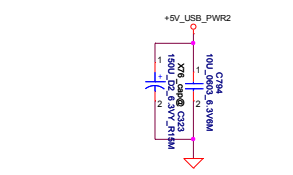
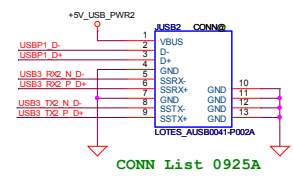
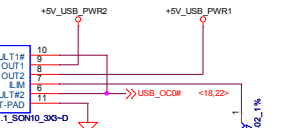
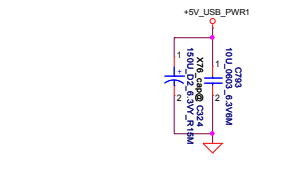
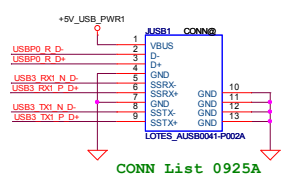
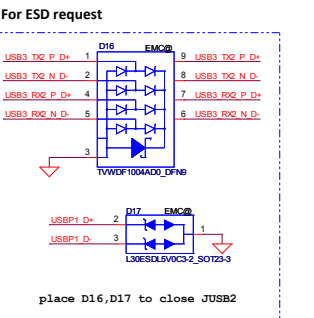
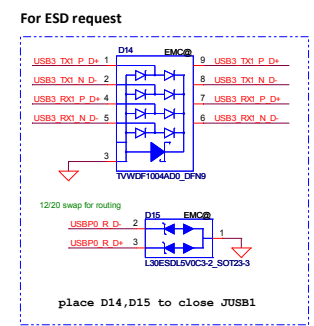
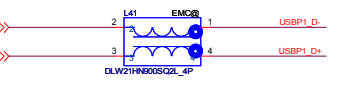
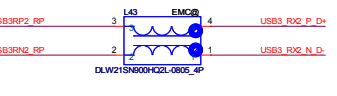
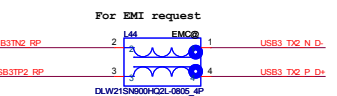
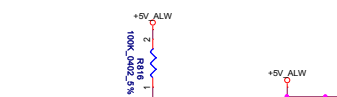
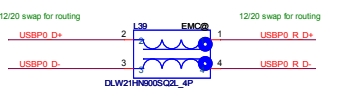
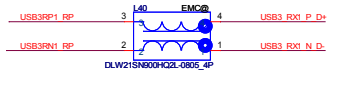
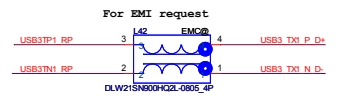
9/9 change main source to SA000064P10(PS8723BTOFN32GTR-A1). <47>

PDR: chip power down, active LOW, 3.3V tolerant.
internally pulled up at ~150K ohm.



CB=0 autodetection charger identification active
CB=1 charging downstream port with active USB2.0 data communication mode with 1.5A support

CB	SELCDP	Function
0	X	DCP autodetect with mouse/keyboard wakeup
1	0	S0 charging with SDP only
1	1	S0 charging with CDP or SDP only (depending on external device)



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USB3.0

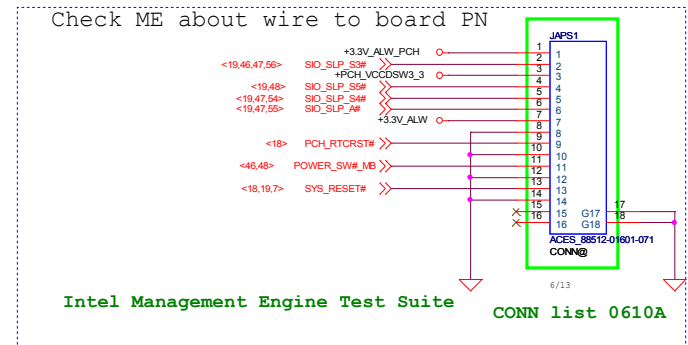
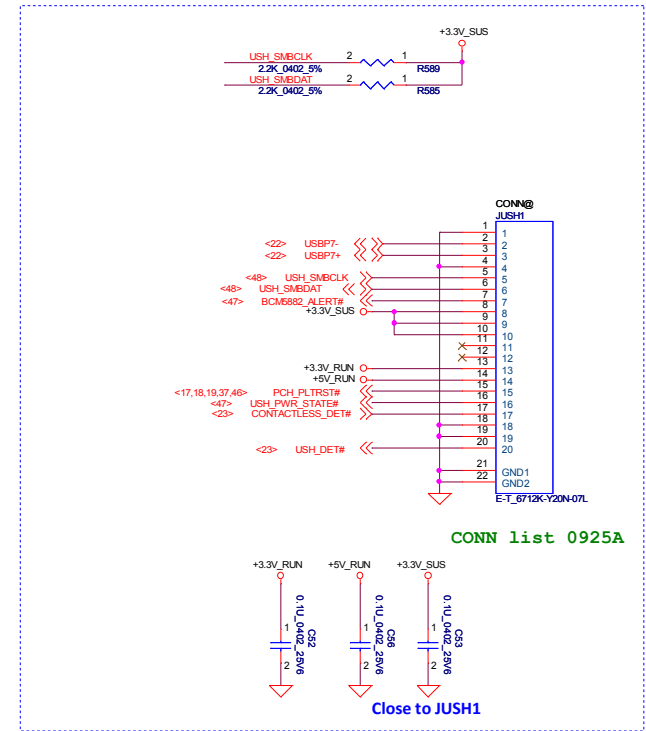
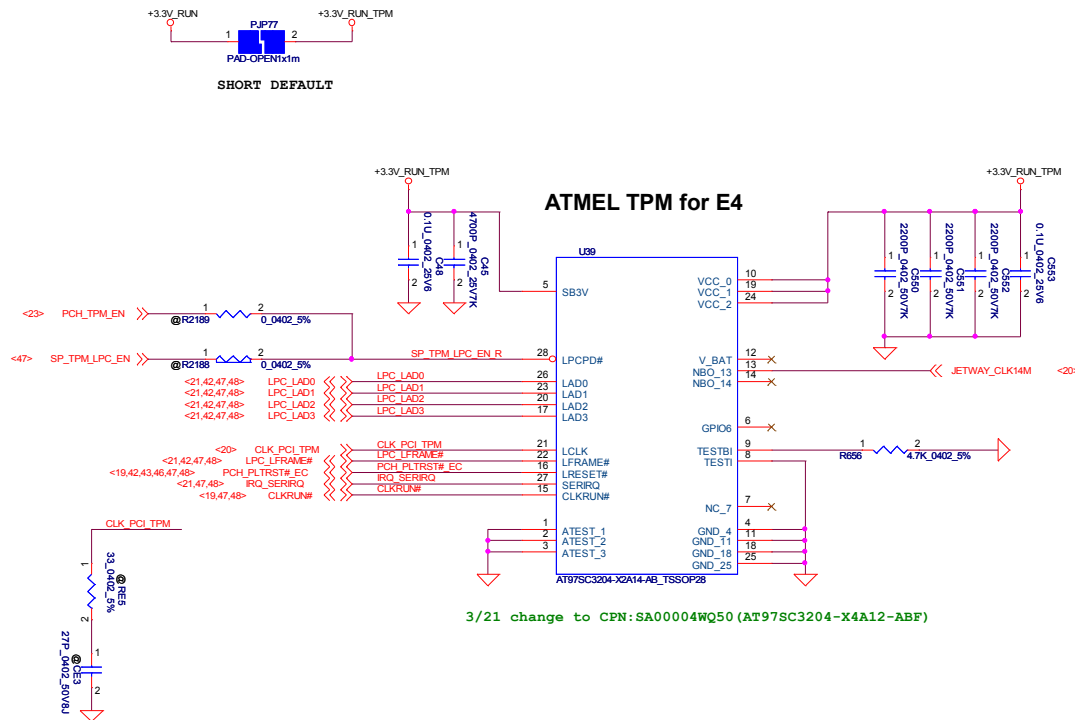
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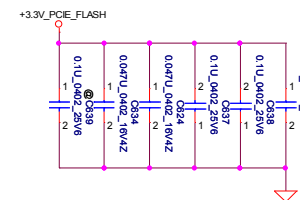
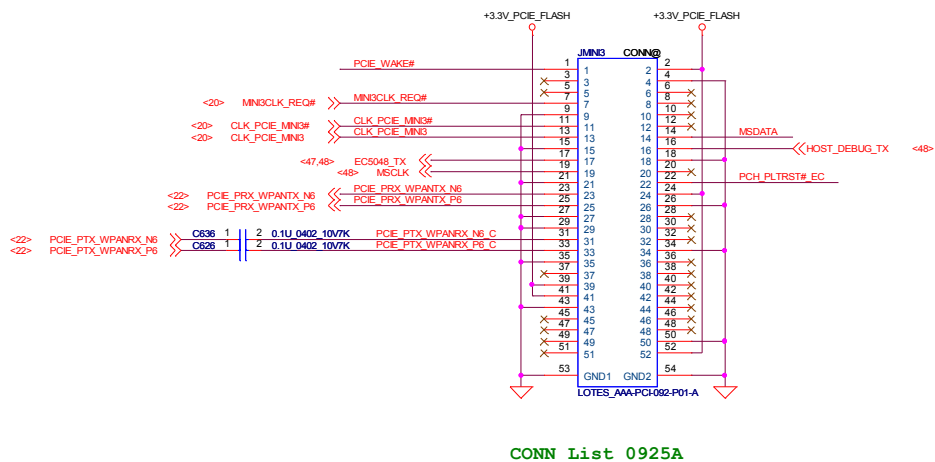
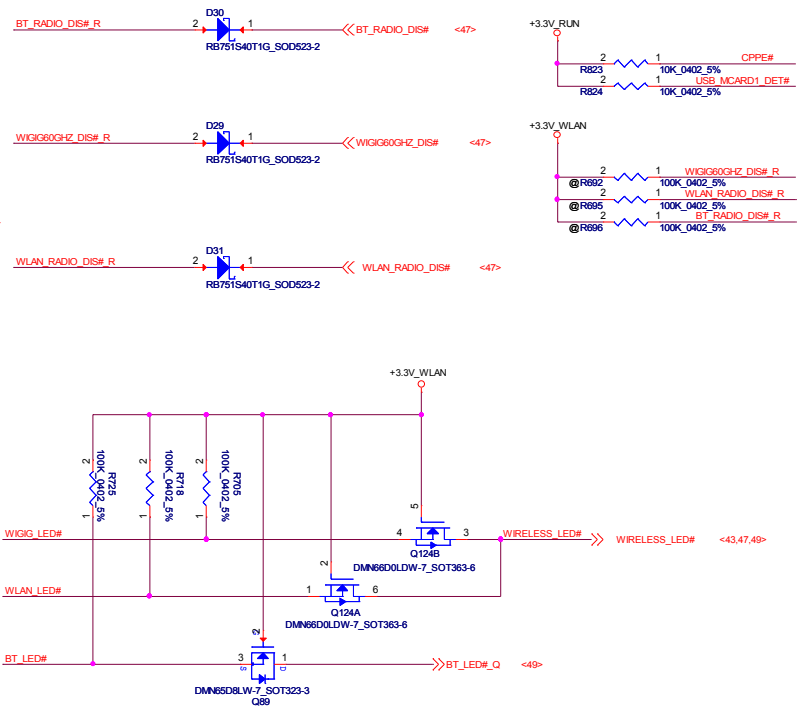
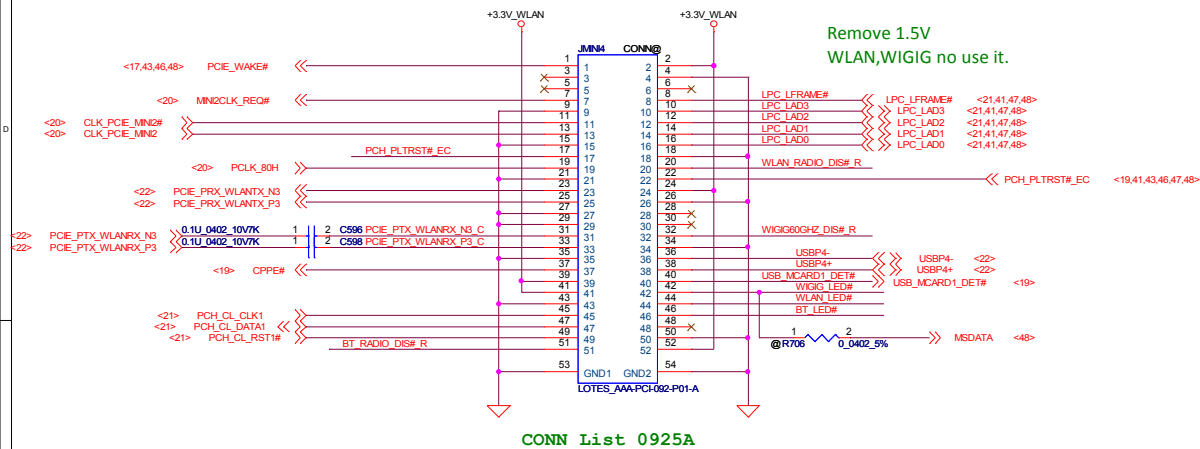
TPM

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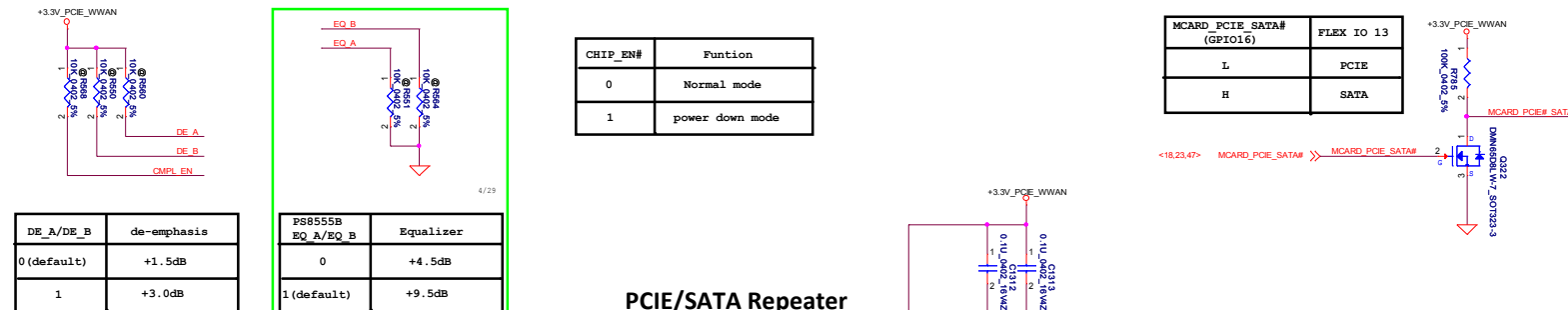
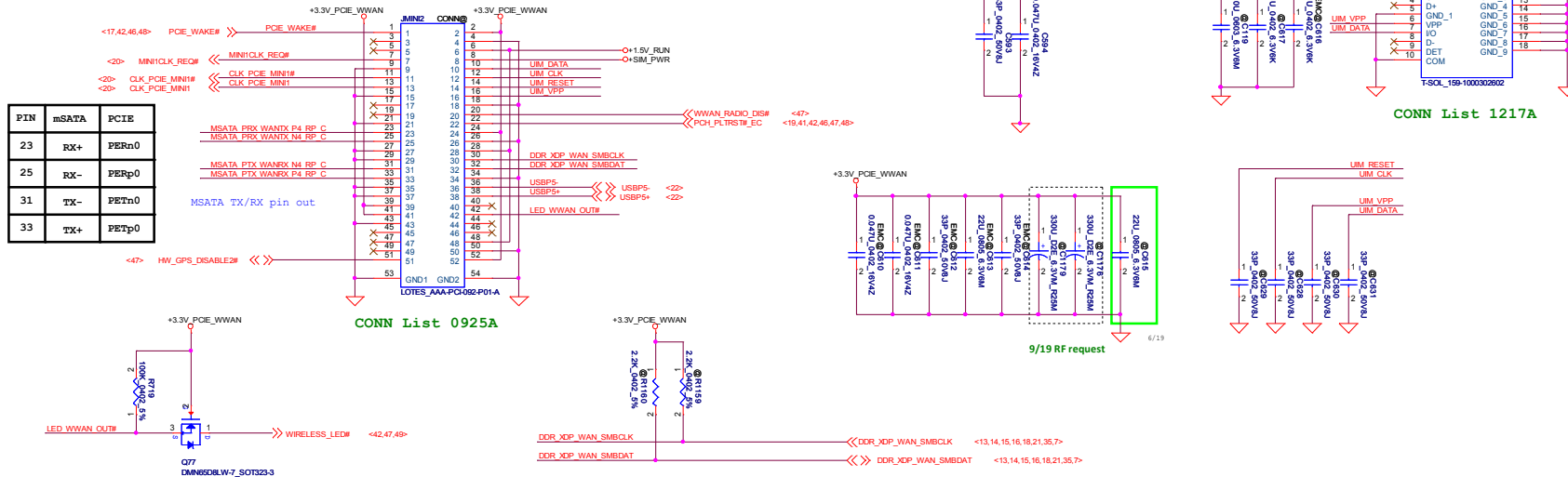
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SIM Card Push-Push

Mini WWAN/GPS/LTE/mSATA



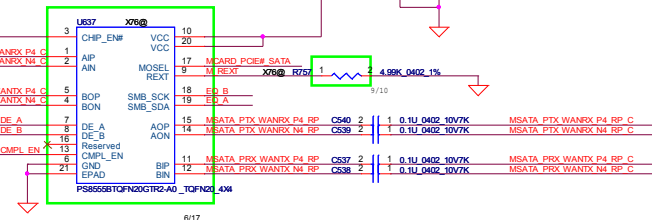
CHIP_EN#	Funtion
0	Normal mode
1	power down mode

MCARD_PCIE_SATA# (GPIO16)	FLEX IO 1
L	PCIE
H	SATA

DE_A/DE_B	de-emphasis
0 (default)	+1.5dB
1	+3.0dB

PS8555B EQ_A/EQ_B	Equalizer
0	+4.5dB
1(default)	+9.5dB

PCIE/SATA Repeater



```
MOSEL 1: PCIE redriver
      0: SATA redriver
```

PCIE/SATA Redriver Select Component

	X76(Main) X7650931L04	X76(2nd) X7650931L03
	PS8555BTQFN20GTR2-A0 SA00006P000	ASM1467 SA000068K00
U637	V	V
R757	V 4.99K(SD034499180)	V 2K(SD034200180)

6/17 change main source to PS8555B(SA00006P000)

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Mini Card-2/2

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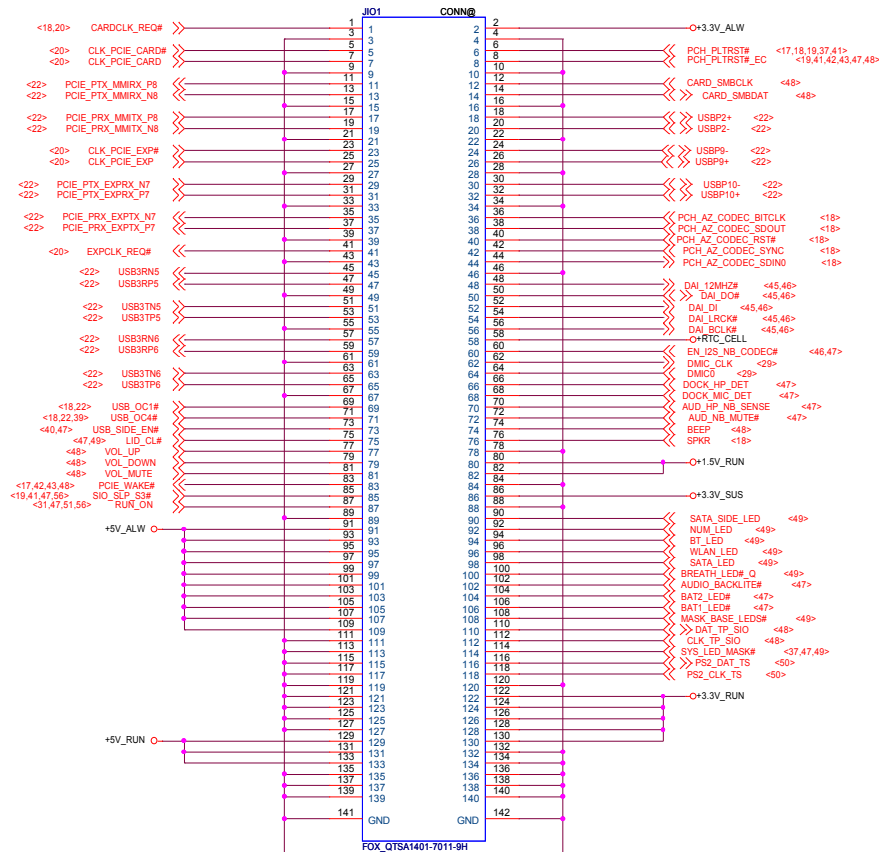
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Size	Document Number	Rev	
	LA-9772P	0.1	
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CONN List 0925A

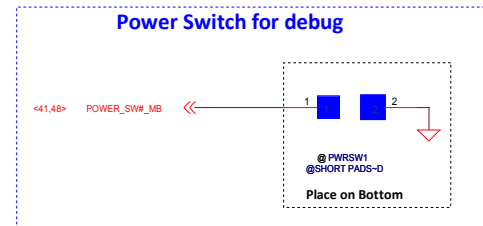
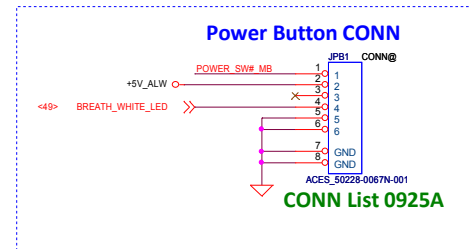
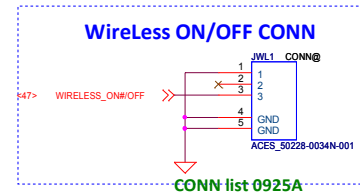
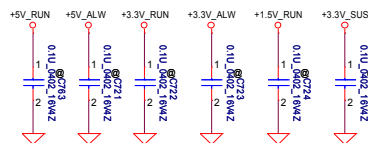


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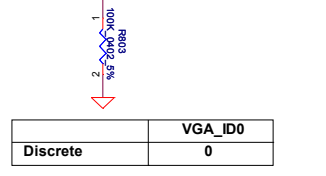
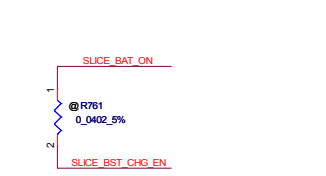
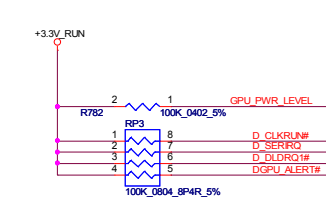
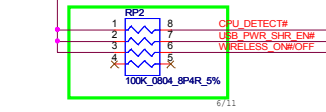
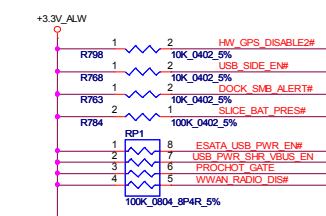
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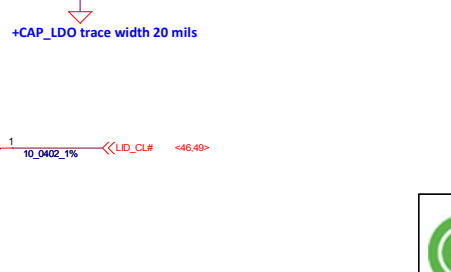
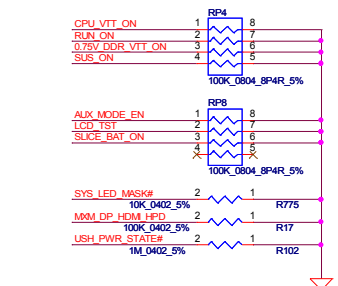
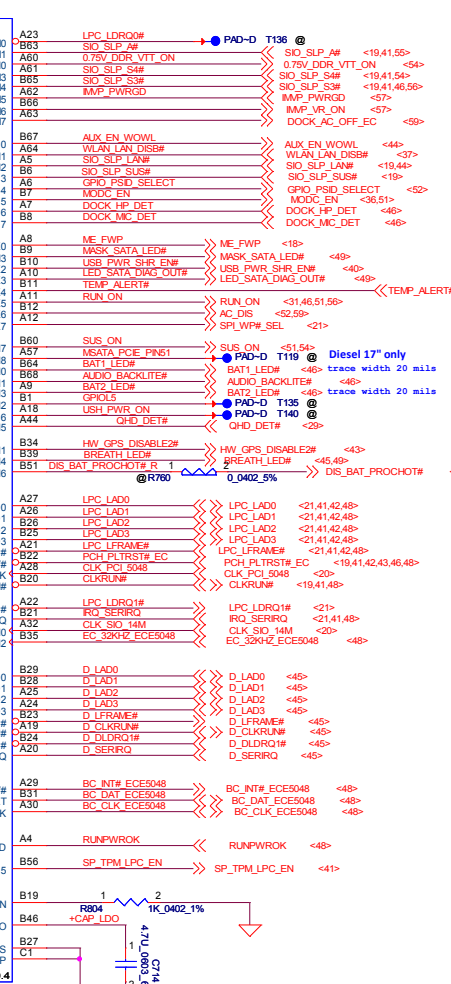
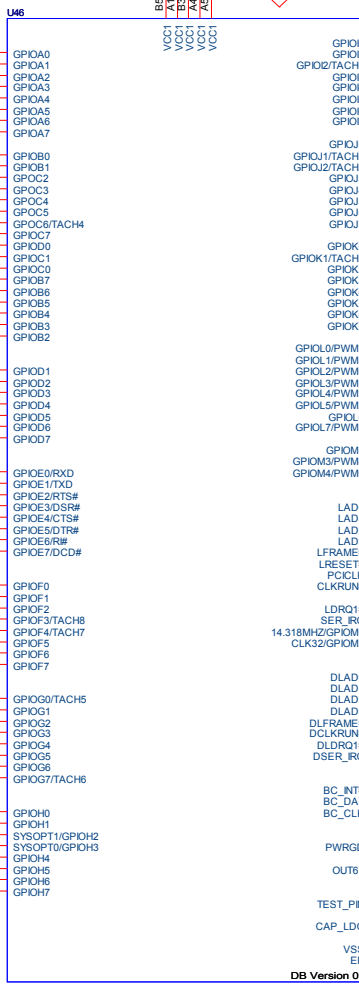
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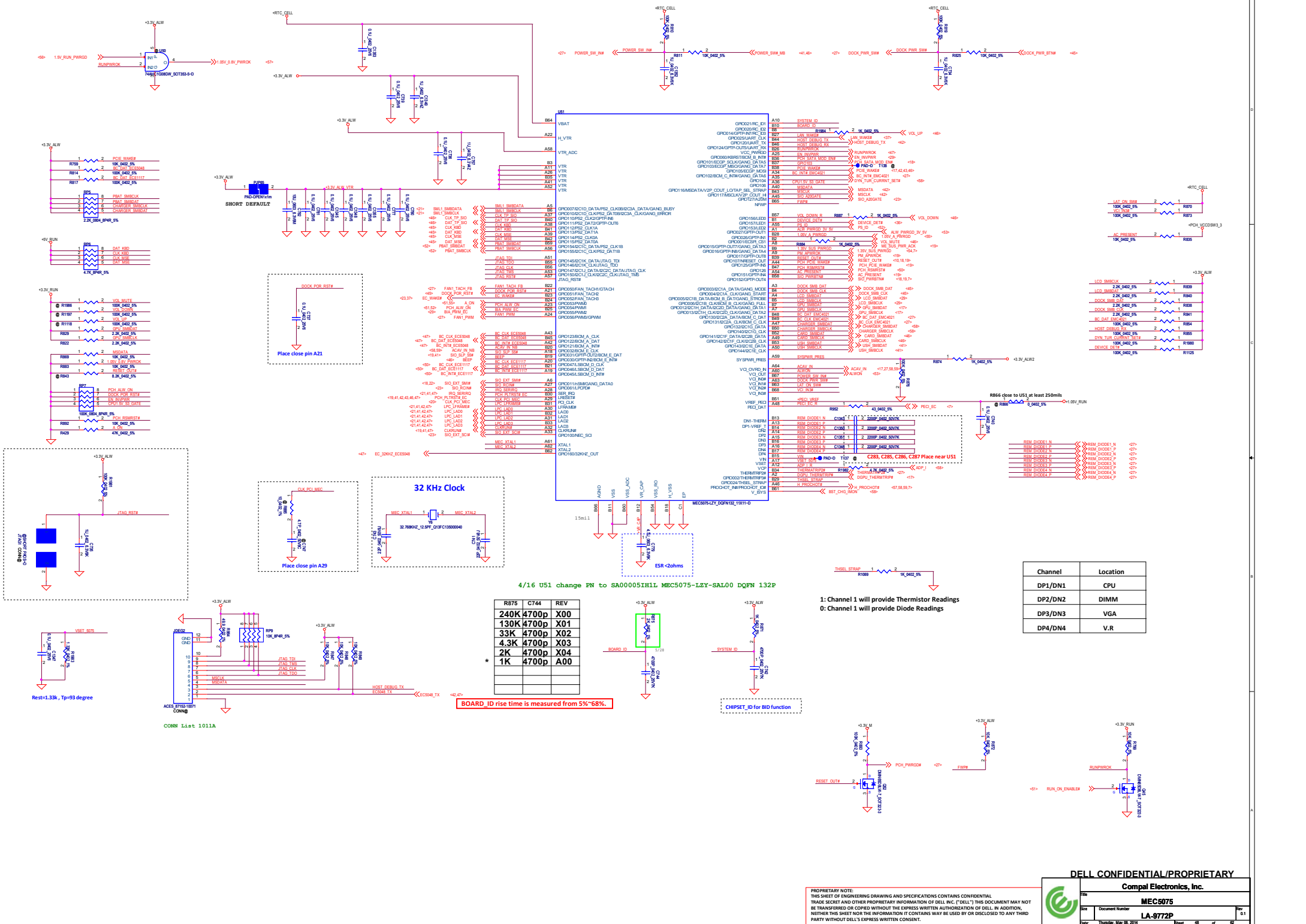


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<31> CRT_SWITCH	<< CRT_SWITCH	B52	GPIOA0	A23	LPC_LDRQ0#	>> PAD-D T136 @	
<54> DDR_1.35V_CNTRL0	<< EN_DS_NB_CODECS#	A49	GPIOA1	B63	SIO_SLP_#	>> SIO_SLP_#	<18,41,55>
<44> MCARD_MSC_PWREN	<< USH_PWR_STATE#	B53	GPIOA2	A60	0.75V_DDR_VTT_ON	>> 0.75V_DDR_VTT_ON	<18,41,55>
<58> PROCHOT_GATE	<< EN_DOCK_PWR_BAR	B54	GPIOA3	A61	SIO_SLP_S4#	>> SIO_SLP_S4#	<18,41,55>
	<< LCD_CL_SIG#	B54	GPIOA4	B65	SIO_SLP_S3#	>> SIO_SLP_S3#	<18,41,55>
<45,52> DOCK_SMB_ALERT#	<< DOCK_SMB_ALERT#	A51	GPIOA5	A62	IMVP_PWRGD	>> IMVP_PWRGD	<57>
@ T155 PAD-D	<< TOUCH_SCREEN_PD#	B55	GPIOA6	B66	IMVP_VR_ON	>> IMVP_VR_ON	<57>
GPU_PWR_LEVEL	<< GPU_PWR_LEVEL	A52	GPIOA7	A63	DOCK_AC_OFF_EC	>> DOCK_AC_OFF_EC	<59>
	<< USB_SIDE_EN#	A33	GPIOB0	B67	AUX_EN_WOWL	>> AUX_EN_WOWL	<44>
<40,46> EN_DS_NB_CODECS#	<< EN_DS_NB_CODECS#	B36	GPIOB1	A64	WLAN_LAN_DISB#	>> WLAN_LAN_DISB#	<37>
<46> USH_PWR_STATE#	<< USH_PWR_STATE#	A34	GPIOC2	B6	SIO_SLP_SUS#	>> SIO_SLP_SUS#	<19,44>
<59> EN_DOCK_PWR_BAR	<< EN_DOCK_PWR_BAR	B37	GPIOC3	A6	GPIO_PSID_SELECT	>> GPIO_PSID_SELECT	<52>
<29> PANEL_BKEN_EC	<< PANEL_BKEN_EC	A35	GPIOC4	A7	MODC_HP_DET	>> MODC_HP_DET	<36,51>
<19,29> ENMOD_PCH	<< ENMOD_PCH	B38	GPIOC5	B8	DOCK_MIC_DET	>> DOCK_MIC_DET	<46>
<29> LCD_TST	<< LCD_TST	A36	GPIOC6	A8	ME_FWP	>> ME_FWP	<18>
<52> PSID_DISABLE#	<< PSID_DISABLE#	A37	GPIOC7	B9	MASK_SATA_LED#	>> MASK_SATA_LED#	<49>
<52,59> PBAT_PRES#	<< PBAT_PRES#	B40	GPIOC8	A10	USB_PWR_SHR_EN#	>> USB_PWR_SHR_EN#	<40>
<45> DOCK_DET#	<< DOCK_DET#	A38	GPIOC9	B10	LED_SATA_DIAG_OUT#	>> LED_SATA_DIAG_OUT#	<49>
<46> AUD_NB_MUTE#	<< AUD_NB_MUTE#	B41	GPIOC10	B11	TEMP_ALERT#	>> TEMP_ALERT#	<21>
@ T127 PAD-D	<< MCARD_WWAN_PWREN	A39	GPIOC11	A11	RUN_ON	>> RUN_ON	<31,46,51,55>
LCD_VCC_TEST_EN	<< LCD_VCC_TEST_EN	B42	GPIOC12	B12	AC_DIS	>> AC_DIS	<52,59>
<29> CCD_OFF	<< CCD_OFF	A40	GPIOC13	A12	SPL_WPW_SEL	>> SPL_WPW_SEL	<21>
<46> AUD_HP_NB_SENSE	<< AUD_HP_NB_SENSE	B43	GPIOC14	B0	SUS_ON	>> SUS_ON	<51,54>
<39> ESATA_USB_PWR_EN#	<< ESATA_USB_PWR_EN#	A44	GPIOC15	A37	MSATA_PCIE_PEN1	>> MSATA_PCIE_PEN1	<51,54>
	<< M/RAM_PWR_EN	B44	GPIOC16	B64	BAT1_LED#	>> BAT1_LED#	<46> trace width 20 mils
<44> M/RAM_PWR_EN	<< M/RAM_PWR_EN	A31	GPIOC17	A9	BAT2_LED#	>> BAT2_LED#	<46> trace width 20 mils
<59> SLICE_BAT_ON	<< SLICE_BAT_ON	B33	GPIOC18	B1	USH_PWR_ON	>> USH_PWR_ON	<46>
<45,52,59> SLICE_BAT_PRES#	<< SLICE_BAT_PRES#	A15	GPIOC19	A44	QHD_DET#	>> QHD_DET#	<2>
<58> BST_CHG_MODE#	<< BST_CHG_MODE#	B16	GPIOC20	B34	HW_GPS_DISABLE2#	>> HW_GPS_DISABLE2#	<45,49>
<3> PBA_GPU_SEL#	<< PBA_GPU_SEL#	A16	GPIOC21	B39	BREATH_LED#	>> BREATH_LED#	<45,49>
<59> SLICE_BST_CHG_EN	<< SLICE_BST_CHG_EN	B16	GPIOC22	B51	DIS_BAT_PROCHOT#	>> DIS_BAT_PROCHOT#	<59>
<54> DDR_1.35V_CNTRL1	<< DDR_1.35V_CNTRL1	A16	GPIOC23				
	<< WIGIG60GHZ_DIS#	A1	GPIOC24	A27	LPC_LAD0	>> LPC_LAD0	<21,41,42,48>
<42> WIGIG60GHZ_DIS#	<< WIGIG60GHZ_DIS#	B2	GPIOC25	A26	LPC_LAD1	>> LPC_LAD1	<21,41,42,48>
<42,48> EC5048_TX	<< EC5048_TX	A2	GPIOC26	B25	LPC_LAD2	>> LPC_LAD2	<21,41,42,48>
<18,23,43> MCARD_PCIE_SATA#	<< MCARD_PCIE_SATA#	B3	GPIOC27	A21	LPC_LAD3	>> LPC_LAD3	<21,41,42,48>
<7> CPU_DETECT#	<< CPU_DETECT#	A3	GPIOC28	B22	LPC_LFRAME#	>> LPC_LFRAME#	<21,41,42,48>
<17,19> DGPU_PWR_EN	<< DGPU_PWR_EN	B45	GPIOC29	A28	POH_PLTRST#_EC	>> POH_PLTRST#_EC	<19,41,42,43,46,48>
<17> DGPU_ALERT#	<< DGPU_ALERT#	A42	GPIOC30	B20	CLK_PCL5048	>> CLK_PCL5048	<20>
<17> MMIO_DP_HDM_HPD	<< MMIO_DP_HDM_HPD	B4	GPIOC31	A22	LPC_LDRQ1#	>> LPC_LDRQ1#	<21>
	<< ZODD_WAKE#	A59	GPIOC32	B21	RQ_SERRIO	>> RQ_SERRIO	<21,41,48>
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<41> BCM6882_ALERT#	<< BCM6882_ALERT#	A58	GPIOC34	B35	EC_32KHZ_ECE5048	>> EC_32KHZ_ECE5048	<48>
<19> SUSACK#	<< SUSACK#	B61	GPIOC35				
<31> EDIO_SELECT#	<< EDIO_SELECT#	A56	GPIOC36				
<17,23> DGPU_PWROK	<< DGPU_PWROK	B59	GPIOC37				
<20,51> 3.3V_RUN_GFX_ON	<< 3.3V_RUN_GFX_ON	A55	GPIOC38				
<23> SLP_ME_CSW_DEV#	<< SLP_ME_CSW_DEV#	B58	GPIOC39				
	<< LAN_DISABLE#_R	B47	GPIOC40				
<37> LAN_DISABLE#_R	<< LAN_DISABLE#_R	A45	GPIOC41				
<37,46,49> SYS_LED_MASK#	<< SYS_LED_MASK#	B48	GPIOC42				
@ T130 PAD-D	<< DYN_TURB_SYS_PWR_ALERT#	A46	GPIOC43				
<18,23> SIO_EXT_WAKE#	<< SIO_EXT_WAKE#	B49	GPIOC44				
<42,43,49> WIRELESS_LED#	<< WIRELESS_LED#	A47	GPIOC45				
<40> USB_PWR_SHR_VBUS_EN	<< USB_PWR_SHR_VBUS_EN	B50	GPIOC46				
<42> WLAN_RADIO_DIS#	<< WLAN_RADIO_DIS#	A48	GPIOC47				
	<< WIRELESS_ON#OFF	B13	GPIOC48				
<46> WIRELESS_ON#OFF	<< WIRELESS_ON#OFF	A13	GPIOC49				
<42> BT_RADIO_DIS#	<< BT_RADIO_DIS#	B57	GPIOC50				
<43> WWAN_RADIO_DIS#	<< WWAN_RADIO_DIS#	A53	GPIOC51				
<19,7> SYS_PWROK	<< SYS_PWROK	B14	GPIOC52				
<19,44> SIO_SLP_WLAN#	<< SIO_SLP_WLAN#	A14	GPIOC53				
<19> PCH_DP_WROK	<< PCH_DP_WROK	B17	GPIOC54				
	<< CPU_VTT_ON	B18	GPIOC55				





4/16 U51 change PN to 8A000051HIL MEC5075-LZY-SAL00 DQPN 132P


R875	C744	REV
240K	4700p	X00
130K	4700p	X01
33K	4700p	X02
4.3K	4700p	X03
2K	4700p	X04
1K	4700p	A00

BOARD_ID rise time is measured from 5%-68%

1: Channel 1 will provide Thermistor Readings
0: Channel 1 will provide Diode Readings

Channel	Location
DP1/DN1	CPU
DP2/DN2	DIMM
DP3/DN3	VGA
DP4/DN4	V.R

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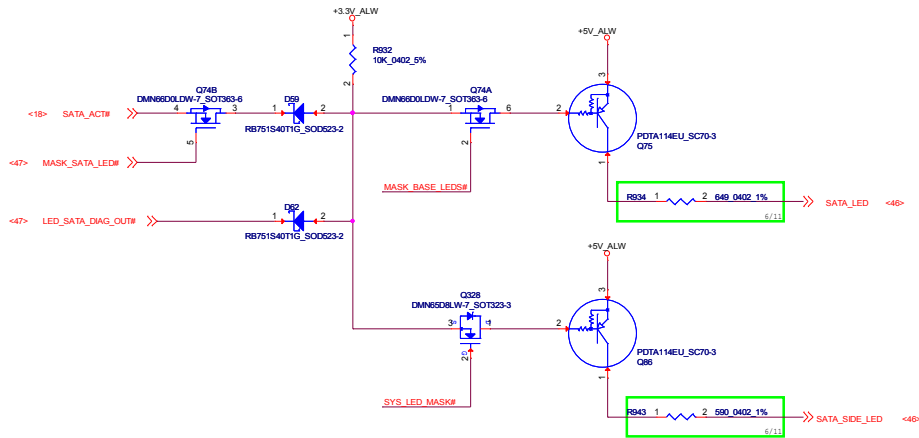


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MEC5075
LA-9772P
Thursday, May 08, 2014

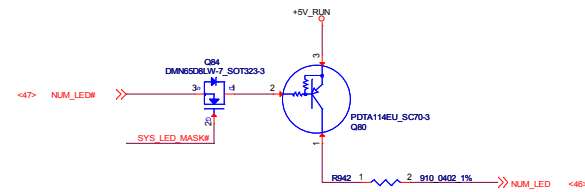
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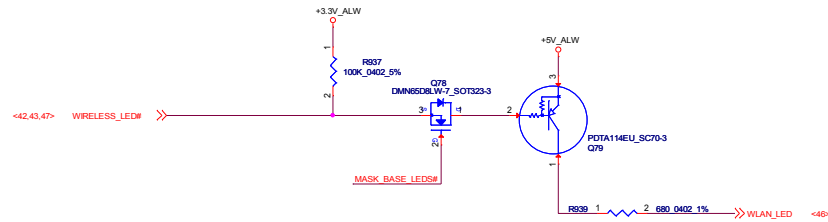
HDD LED



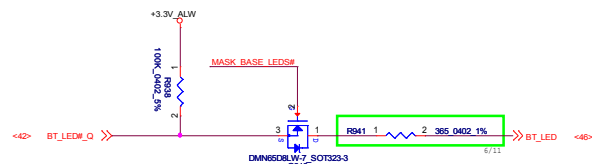
NUM LED



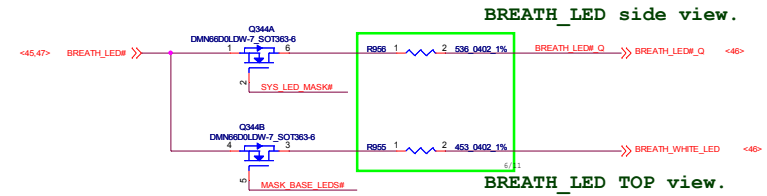
WWAN/WLAN LED



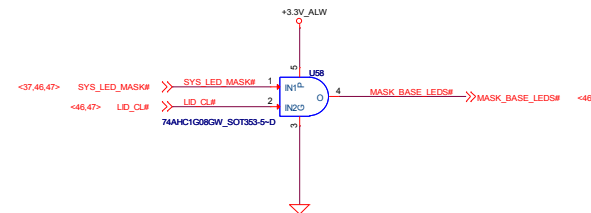
BT LED



Breath LED

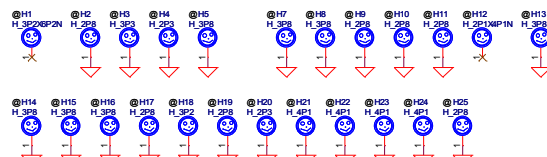


LED Circuit Control Table		
	SYS_LED_MASK#	LID_CL#
Mask All LEDs (Sniffer Function)	0	X
Mask Base MB LEDs (Lid Closed)	1	0
Do not Mask LEDs (Lid Opened)	1	1



Fiducial Mark

- FD1
- FIDUCIAL MARK-D
- FD2
- FIDUCIAL MARK-D
- FD3
- FIDUCIAL MARK-D
- FD4
- FIDUCIAL MARK-D



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PAD & Standoff & LED

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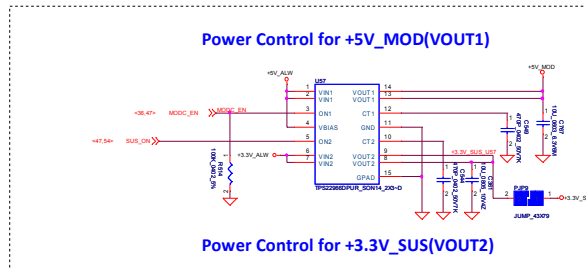
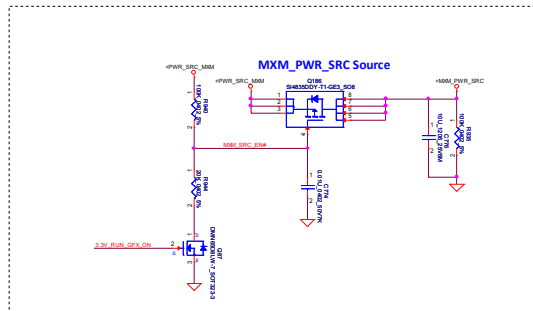
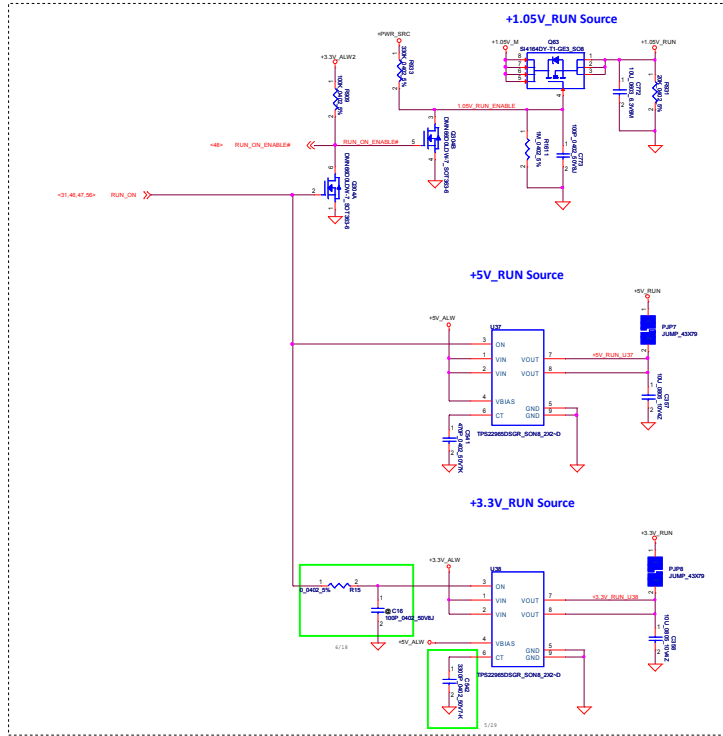
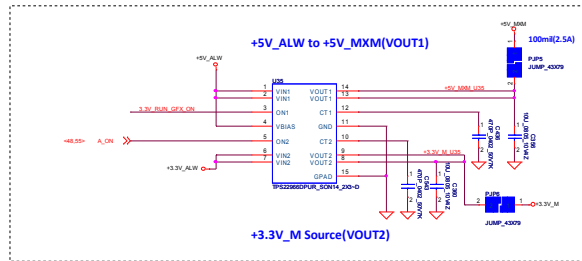
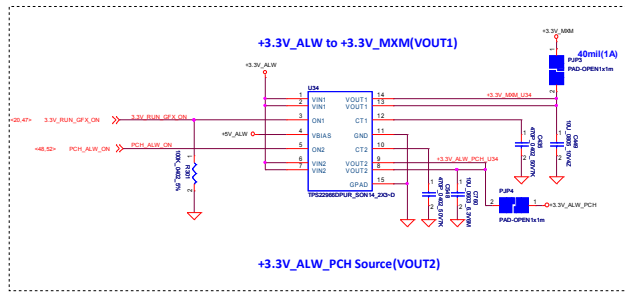
RSMRST circuit

change to CPN:SA00005A600(RT9181A-44GU3_SC70-3)

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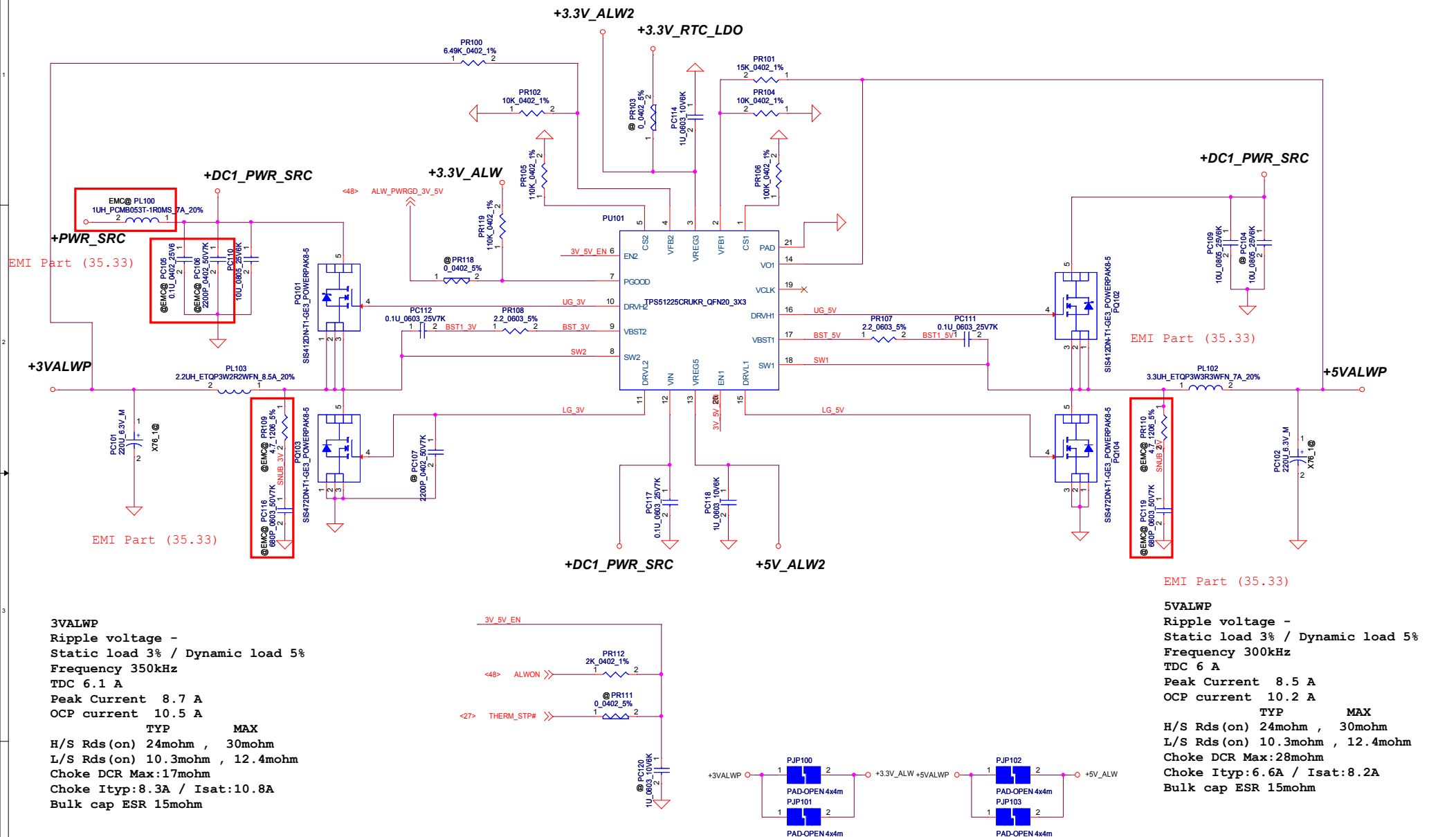
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Power Control

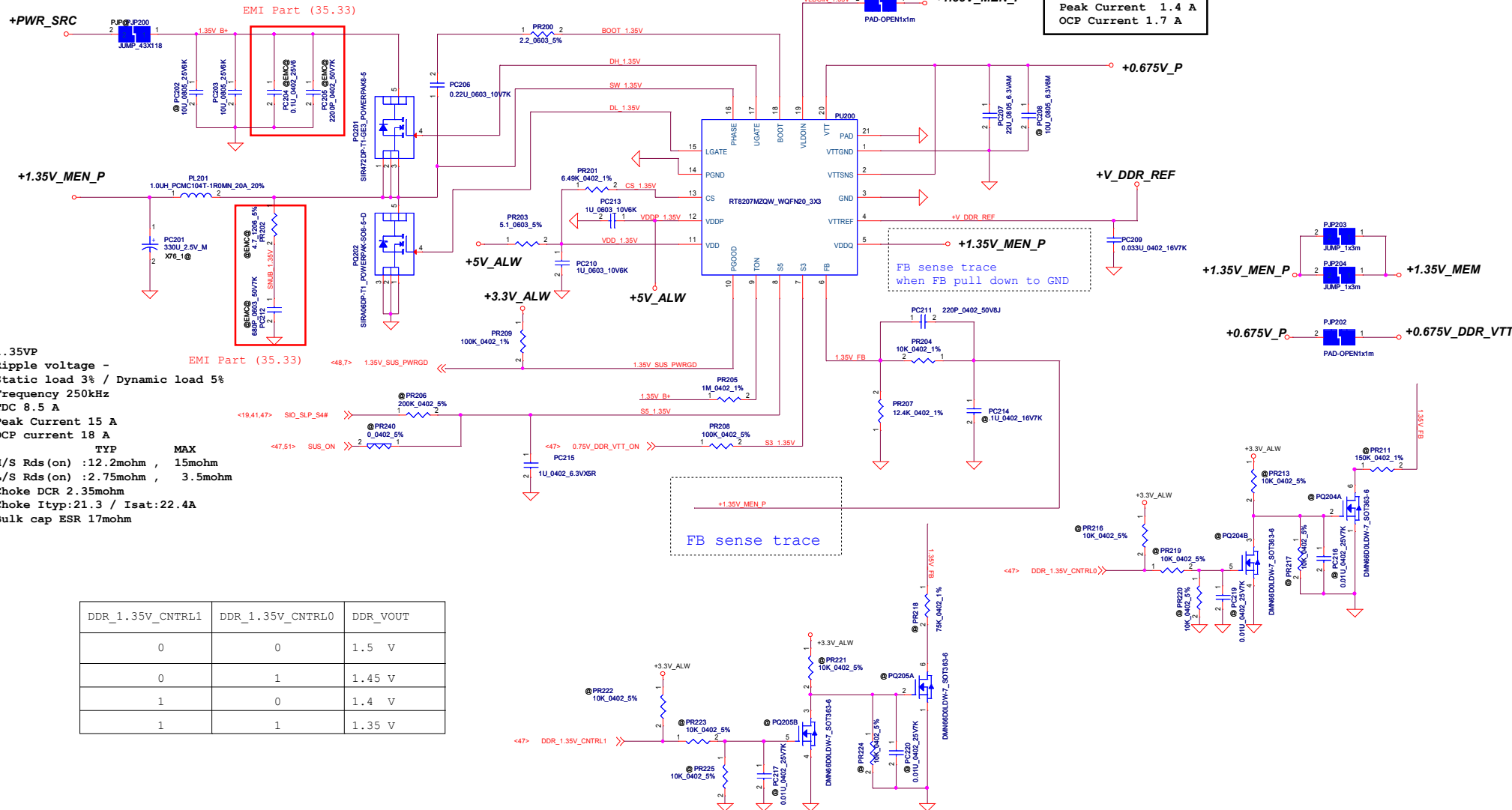
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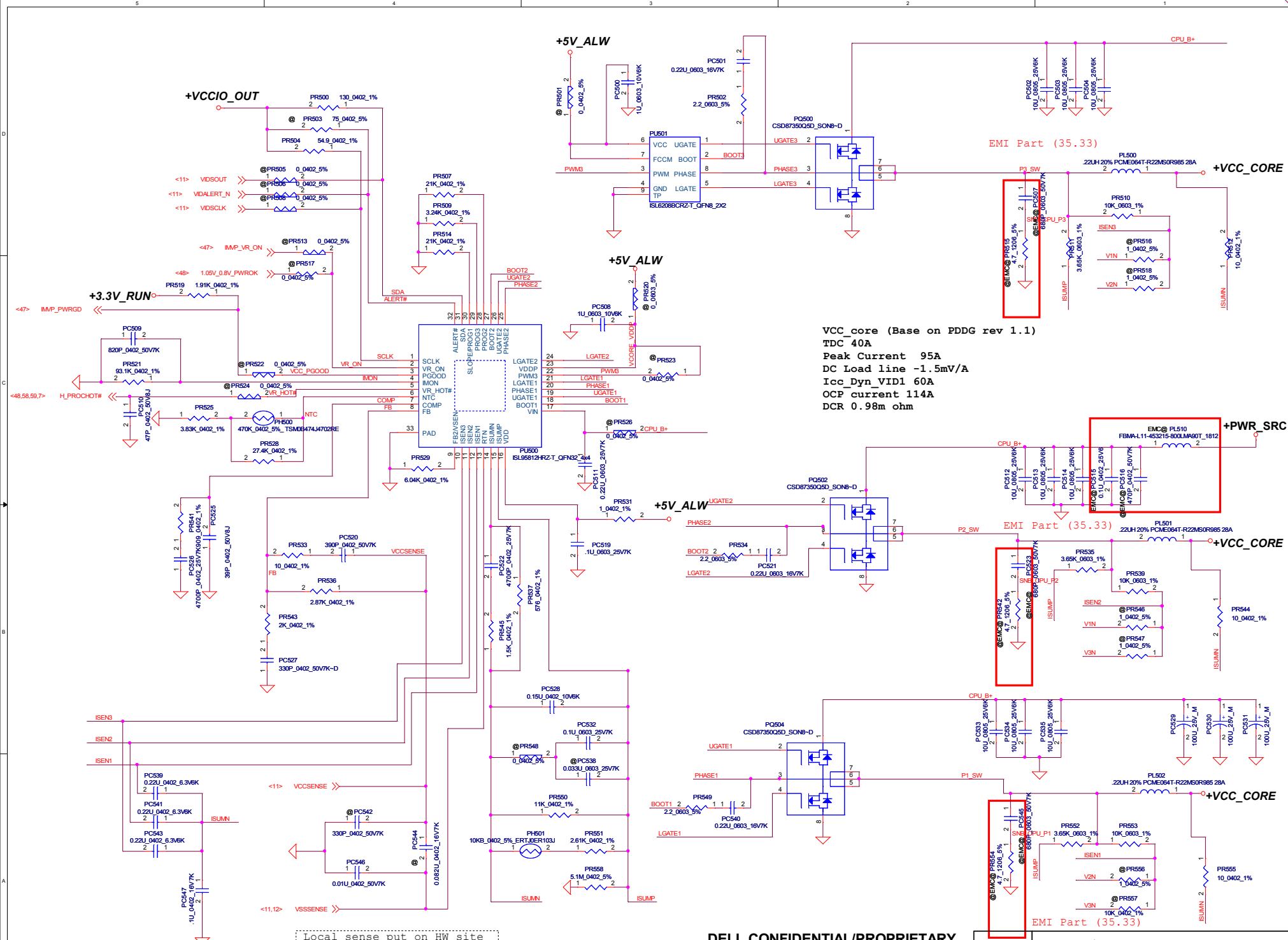
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VCC_core (Base on PDDG rev 1.1)
TDC 40A
Peak Current 95A
DC Load line -1.5mV/A
Icc Dyn_VID1 60A
OCP current 114A
DCR 0.98m ohm

Local sense put on HW site

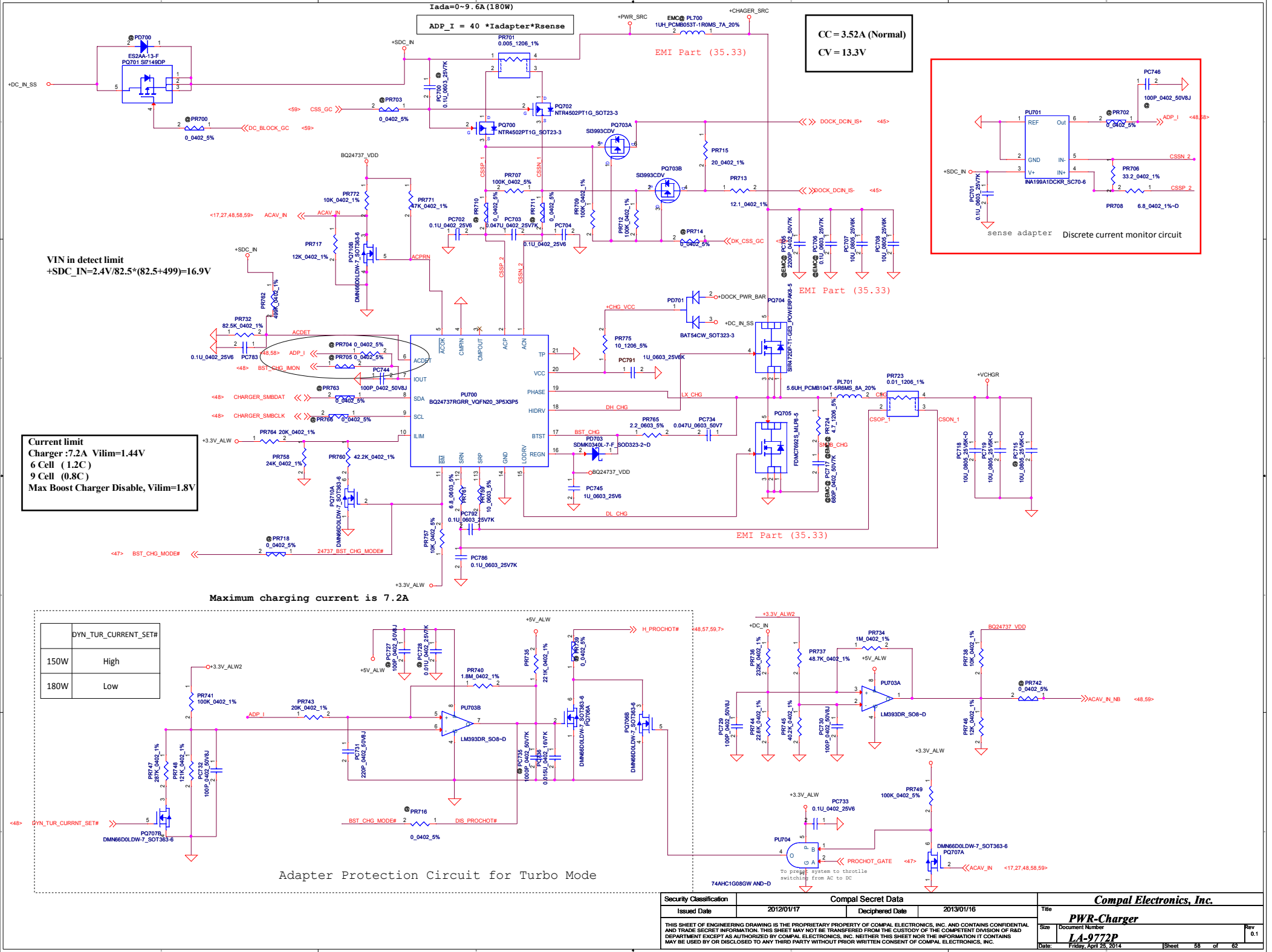
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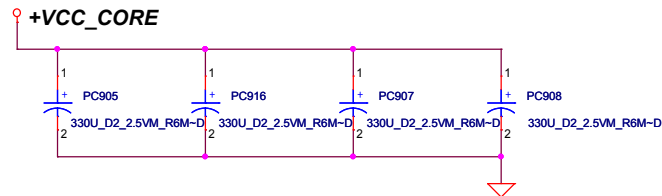
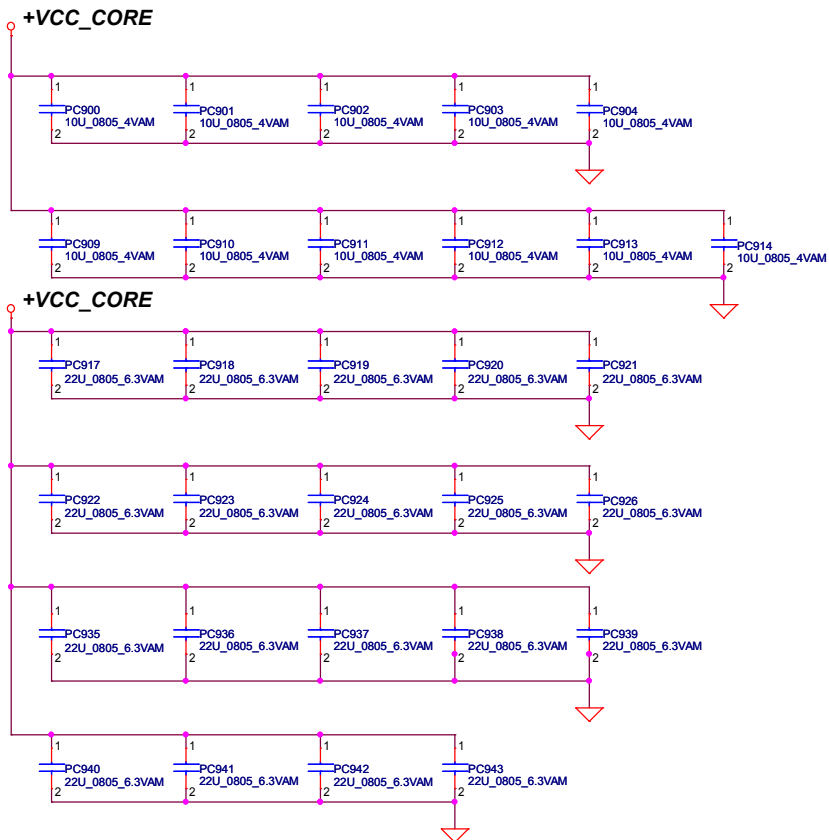


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+VCC_CORE			
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Based on PDDG rev 0.7 Table 5-1.



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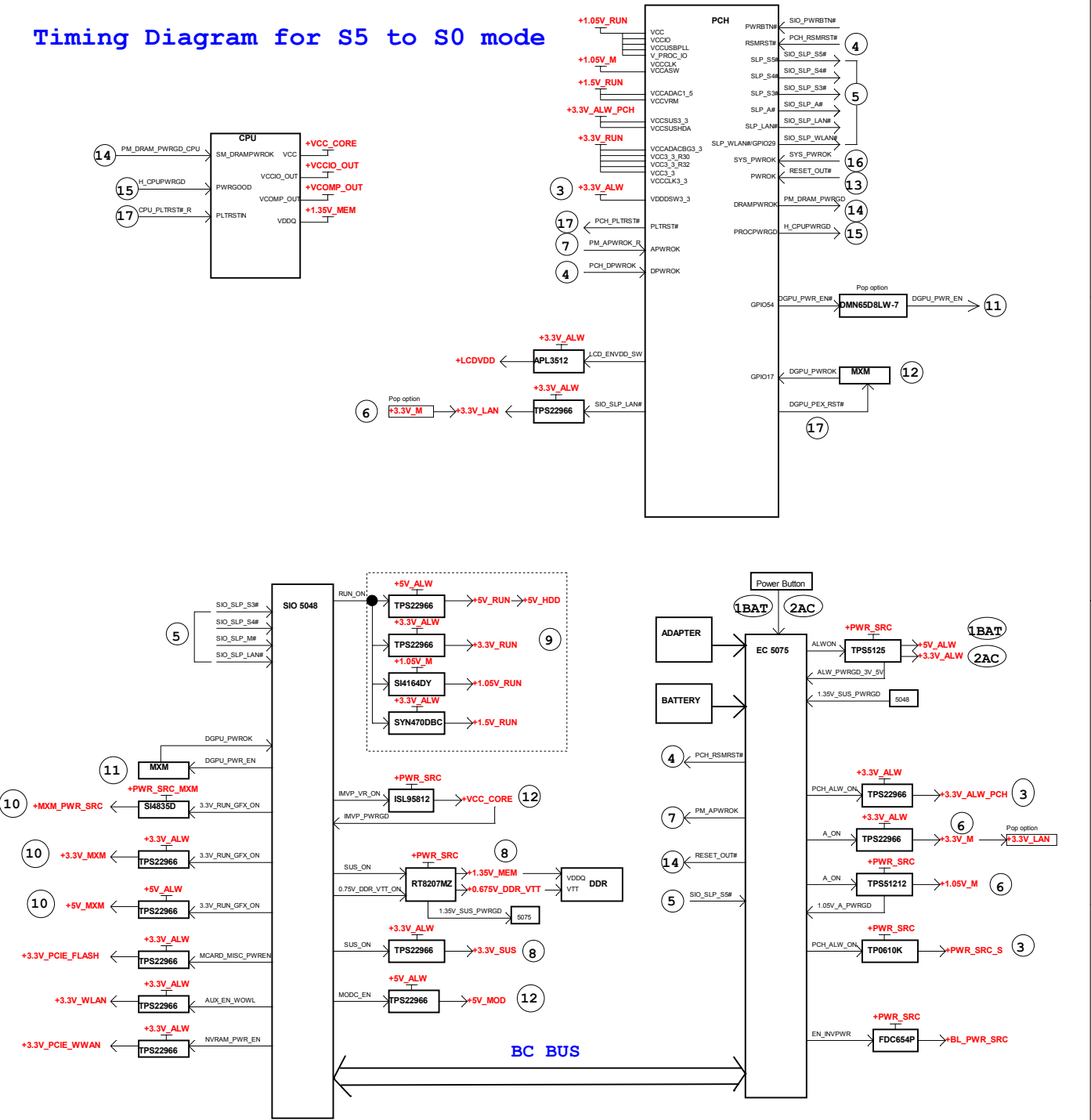
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Timing Diagram for S5 to S0 mode




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